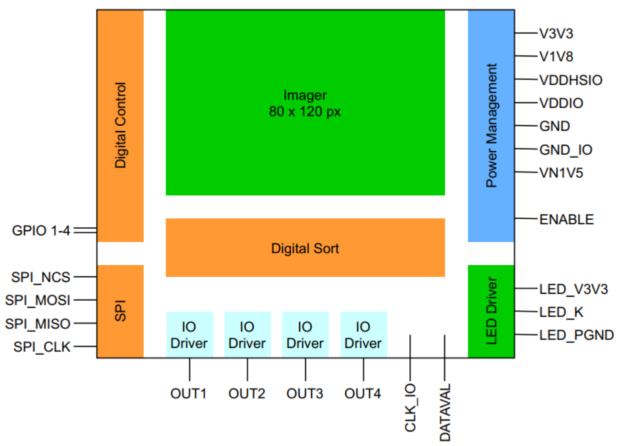
AISC110C 80x120 Pixel Ultra High-Speed Imager

General description

The AISC110C "Cheetah" is a 80x120 high-speed imager. The total image read and digitize time is 24us. For an exposure interval time of 25us, the frame rate is 40k frames/sec. By reducing the active imager array size, frame rates up to 260k frames/sec can be reached. Each pixel is converted to an 8-bit digital signal and send via proprietary parallel interfaces. The exposure time can be controlled from outside or set inside via SPI. For video exposure the imager can be set to continues exposure where the interval can be set by SPI. Integrated PLL is running at 100MHz and is syncing the high-speed I/O. For the high-speed interface drivers there is a separate voltage regulator implemented. The Integrated LED driver can support up to 40mA LED's using current and PWM control. For higher LED drive requirements, the internal generated PWM can be used to drive an external driver.

Block Diagram



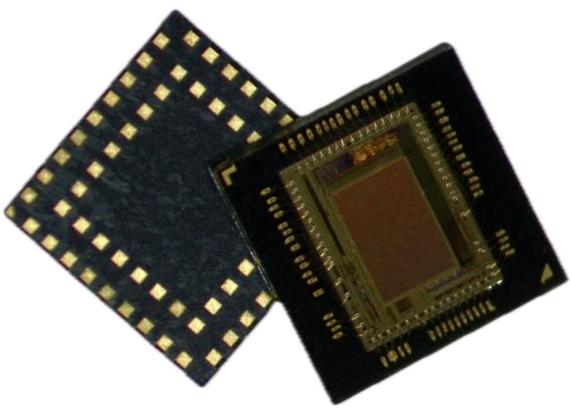
Features

- 80x120 ultra high-speed imager
  - Power down mode
  - High IR sensitivity (>70%QE@850nm)
- Charge-sensor pixel imager
  - Direct pixel charge processing
  - Charge to digital conversion
- OLGA 64 package with an optical window
- SPI Interface
- 4 High-Speed 8-bit parallel digital I/Os for pixel data output (32 I/Os total)
- On board power management
- Single 3.3V external power supply needed
- On board Oscillator and PLL
- LED driver supporting internal and external PWM control
- PWM driver for generating external negative bias voltage
- Four configurable GPIO's

Applications

- Gamer mouse frontend
- High-speed tracking
- High-speed inspection

Package Illustration



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1 Pin Description

Table 1: Pin Description

Pin number	Pin name	Voltage rating	Type	Description
1	SPI_NCS	VDDIO	IN	SPI chip-select not
2	SPI_MOSI	VDDIO	IN	SPI MOSI
3	SPI_CLK	VDDIO	IN	SPI clock input
4	DATAVAL	VDDHSIO	OUT	Synchronization data output
5	OUT1_1	VDDHSIO	OUT	High-speed I/O output
6	OUT1_3	VDDHSIO	OUT	High-speed I/O output
7	OUT1_5	VDDHSIO	OUT	High-speed I/O output
8	OUT1_7	VDDHSIO	OUT	High-speed I/O output
9	OUT2_0	VDDHSIO	OUT	High-speed I/O output
10	SPI_MISO	VDDIO	OUT	SPI MISO
11	GND	0	GND	GND
12	GND_IO	0V	GND	High-speed I/O ground connection
13	OUT1_0	VDDHSIO	OUT	High-speed I/O output
14	OUT1_2	VDDHSIO	OUT	High-speed I/O output
15	OUT1_4	VDDHSIO	OUT	High-speed I/O output
16	OUT1_6	VDDHSIO	OUT	High-speed I/O output
17	OUT2_1	VDDHSIO	OUT	High-speed I/O output
18	OUT2_2	VDDHSIO	OUT	High-speed I/O output
19	OUT2_3	VDDHSIO	OUT	High-speed I/O output
20	OUT2_4	VDDHSIO	OUT	High-speed I/O output
21	OUT2_6	VDDHSIO	OUT	High-speed I/O output
22	OUT2_7	VDDHSIO	OUT	High-speed I/O output
23	CLK_IO	VDDHSIO	OUT	100MHz sync clock for data output
24	OUT3_1	VDDHSIO	OUT	High-speed I/O output
25	OUT3_3	VDDHSIO	OUT	High-speed I/O output
26	OUT3_4	VDDHSIO	OUT	High-speed I/O output
27	VDDHSIO	1.8V	SUPPLY	Regulated 1.8V supply
28	OUT2_5	VDDHSIO	OUT	High-speed I/O output
29	VDDHSIO	1.8V	SUPPLY	Regulated 1.8V supply
30	GND_IO	0V	GND	High-speed I/O ground connection
31	OUT3_0	VDDHSIO	OUT	High-speed I/O output
32	OUT3_2	VDDHSIO	OUT	High-speed I/O output
33	OUT3_5	VDDHSIO	OUT	High-speed I/O output
34	OUT3_7	VDDHSIO	OUT	High-speed I/O output
35	OUT4_1	VDDHSIO	OUT	High-speed I/O output
36	OUT4_3	VDDHSIO	OUT	High-speed I/O output
37	OUT4_5	VDDHSIO	OUT	High-speed I/O output
38	OUT4_7	VDDHSIO	OUT	High-speed I/O output
39	VN1V5	-1.5V	NEG SUPPLY	IC main negative supply
40	CP_SW	V1V8_D	OUT	Clock for external Charge-Pump circuit

41	LED_K	3.3V	ANALOG I/O	LED driver cathode input
42	OUT3_6	VDDHSIO	OUT	High-speed I/O output
43	OUT4_0	VDDHSIO	OUT	High-speed I/O output
44	OUT4_2	VDDHSIO	OUT	High-speed I/O output
45	OUT4_4	VDDHSIO	OUT	High-speed I/O output
46	OUT4_6	VDDHSIO	OUT	High-speed I/O output
47	GND_IO	0V	GND	High-speed I/O ground connection
48	GND	0	GND	GND
49	LED_V3V3	3.3V	SUPPLY	LED driver power supply
50	LED_PGND	0V	GND	Power ground for the LED driver
51	V3V3	3.3V	SUPPLY	Main power supply
52	V1V8_M	1.8V-5V	SUPPLY	EFUSE supply, connect to V3V3
53	V1V8_D	1.8V	SUPPLY	Digital supply, connect to V1V8
54	IMG_V1V8	1.8V	SUPPLY	Imager supply, connect to V1V8
55	GPIO3	VDDIO	IN/OUT	General purpose I/O 3
56	FTM	1.8V-3.3V	IN	Connect to GND in application
57	ENABLE	1.8V-3.3V	IN	Global IC enable
58	VDDIO	1.8V-3.3V	SUPPLY	I/O voltage
59	V3V3	3.3V	SUPPLY	Main power supply
60	V1V8	1.8V	SUPPLY	Regulator output
61	GND	0	GND	GND
62	GPIO4	VDDIO	IN/OUT	General purpose I/O 4
63	GPIO2	VDDIO	IN/OUT	General purpose I/O 2
64	GPIO1	VDDIO	IN/OUT	General purpose I/O 1

Package Pinout

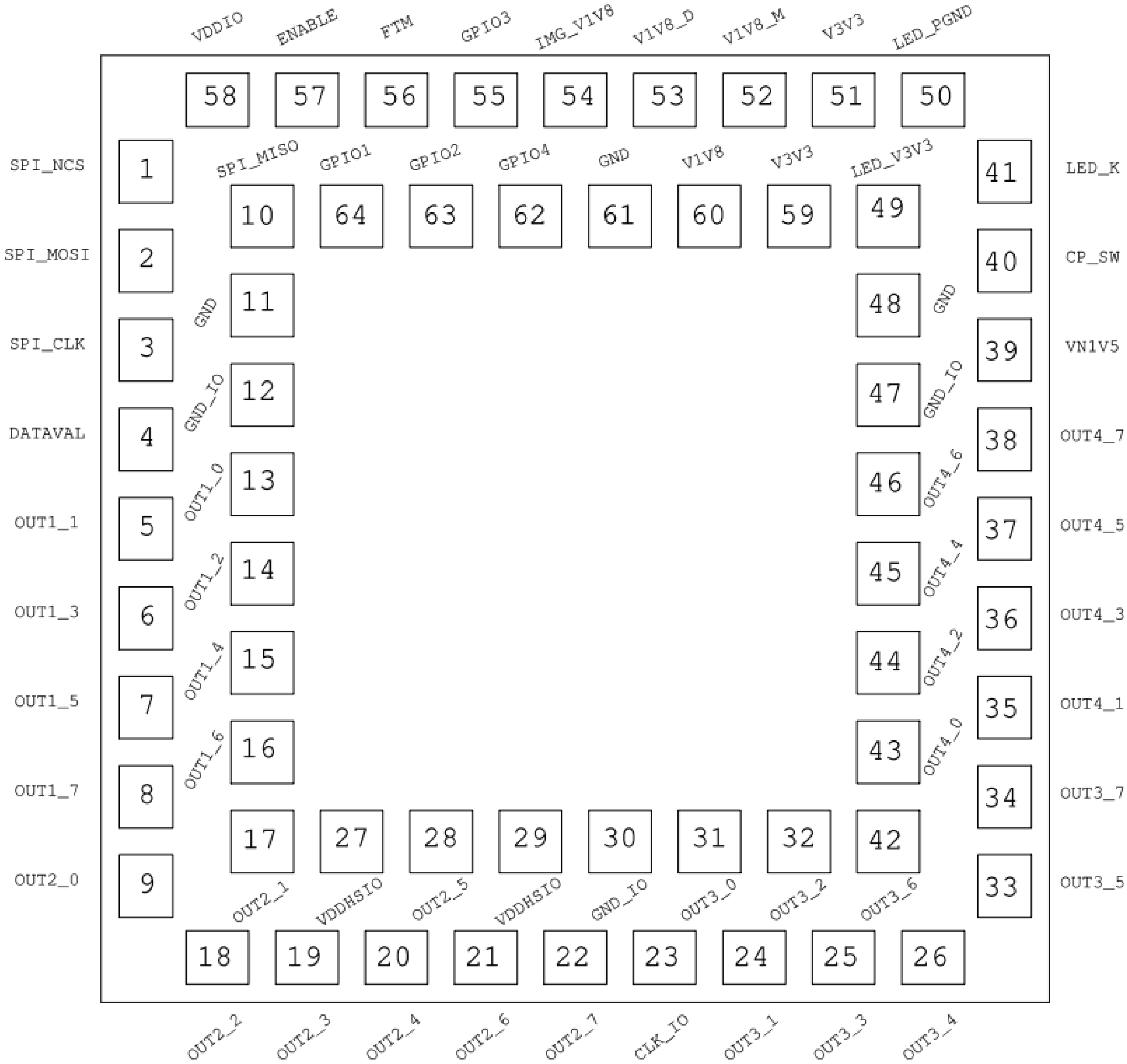


Figure 1: C110C Package Pinout (top view)

2 Detailed Description

C110C is a high-speed imager with full external control. For external control, Exposure and Imager functions can be mapped to GPIO pins. Exposure time and internal restart of exposure can be set via SPI over a wide range. The readout of the imager takes 24us for 8-bit data of 9600 pixels. C110C contains a LED driver for visual and UV light, two internal 1.8V LDO, and several configuration settings. With an external exposure signal, the Pixel exposure time can be set and after the falling edge of the exposure signal the data converted to 8-bit digital is muxed out via 32 I/O pins at a clock speed of 100MHz. By internal PLL, internal CLK can be programmed to achieve different timings. The external receiver can capture the pixel data on the rising edge of the CLK_IO signal when the DATA_VALID signal is high. To reduce the number of parallel I/O pins and the associated power dissipation, a 4-bit data mode can also be programmed, where four 4-bit pixel data is read out via two 8-bit outputs using only 16 pins instead of 32. Using an internal PLL, the internal CLK can be programmed to achieve different timings. There is a general ENABLE pin for power up the device. During ENABLE low, the device is not consuming any power. The LED driver, current limit can be set via SPI after power-up of the device.

2.1 Block Diagram

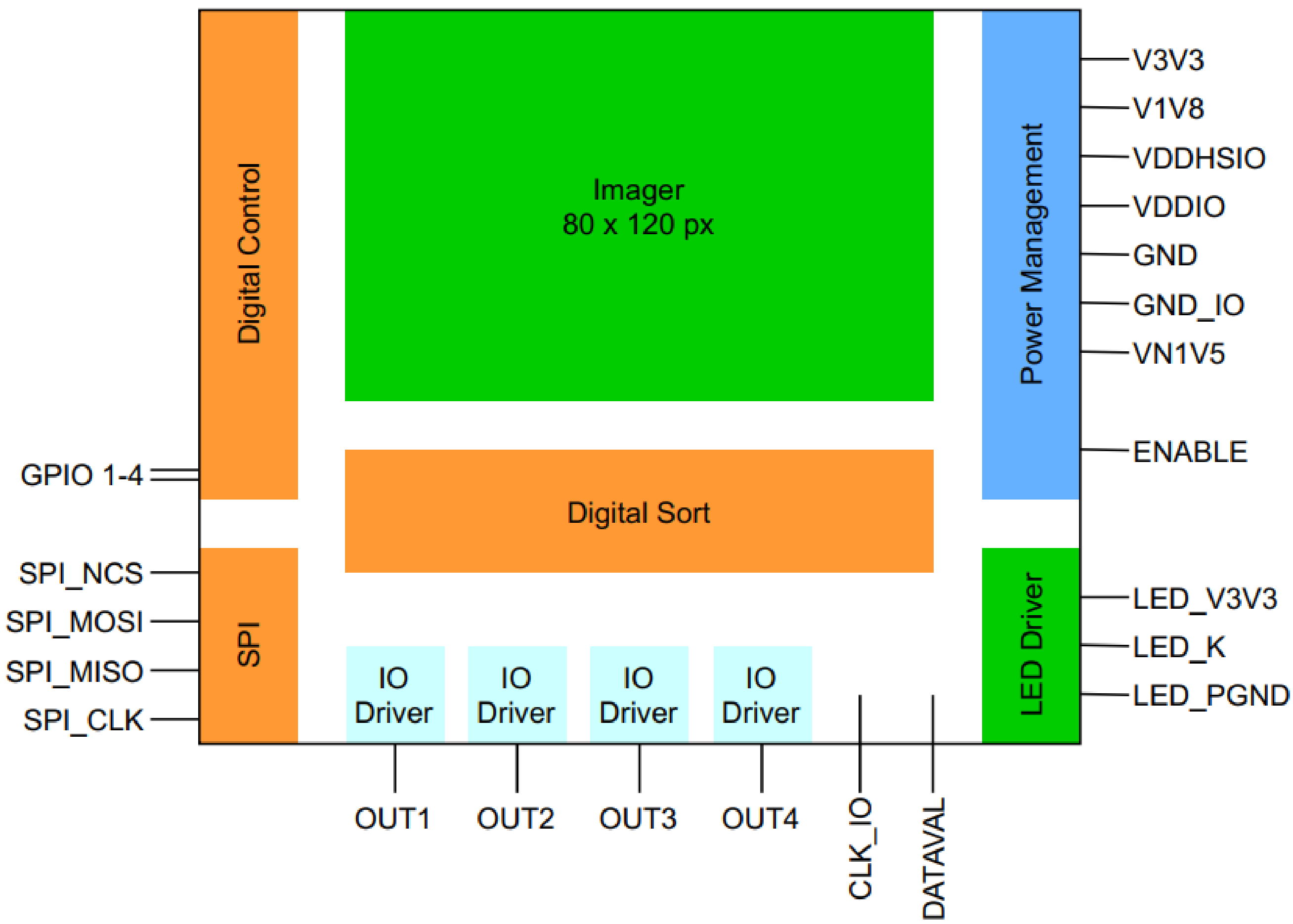


Figure 2: Block Diagram

2.2 Operation

Once the Power-on-Reset (POR) is de-asserted, Cheetah loads the trim data from the eFuse memory. After the data is loaded into the register bank, it signals back a ready towards the micro controller indicating that it's ready for operation.
Once the startup is completed, the micro controller can start the operation by configuring the device and enable the selected operation via SPI register access. When internal exposure is used, the device supports single exposure and continuous exposure. The internal exposure length as well as the continuous exposure periodicity are defined in the corresponding configuration registers. The internal exposure can be started by register access or by an external trigger pulse through one of the GPIOs. Alternatively, the exposure signal can be driven from an external source through the GPIOs, in which case the whole operation is manual and the register settings for the internal exposure generation are ignored.
Cheetah detects the start and the end of the exposure and controls the analog pixel array to capture the image and perform the read-out sequence line by line. At the end of each line's readout sequence, it also starts the TDCs in the analog block, which then provide the digital pixel data for a whole line every 200ns (80 pixels per line) or 100ns (40 pixels per line). The data received from the TDCs are directly multiplexed out onto the synchronous parallel data interface. Depending on the selected pixel accuracy, either the full pixel-data or only the four most significant bits are transmitted for four consecutive pixels on the rising edge of the 100MHz IO clock. In this way, half of the parallel interface data output pads can be saved by opting for a lower pixel accuracy. Once a pre-defined number of images have been processed and transferred, an optional interrupt is generated through the GPIOs.
Cheetah provides various timers and configurable frequency dividers to comply with the analog requirements such as the ramp up time needed to turn on some analog modules before the actual exposure is applied. It also generates a configurable clock for the charge pump and a PWM signal for the LED with different frequency and duty cycle options.
Although Cheetah is mainly a high-speed imager with performance in mind, some power saving options are available. The most significant power saving is achieved by disabling the analog blocks and the 100MHz PLL between two exposures.

2.3 High Speed Imager

To capture an image, the exposure signal is controlling the exposure time. During exposure low, every photodiode is in reset mode and cannot capture any photo current. After exposure signal high, reset is released line by line with 200ns delay/line. Every photodiode is capturing photocurrent. At the end of the exposure time, the photo current is read out (spill and fill) to the charge-based readout circuit and within 100ns translated to an 8-bit digital signal. The 80 pixels/line digitized to 8-bit data is read out in 10ns slices (total 200ns/line) via the 32 I/O drivers. A constant stream of data is performed until the whole imager data is send to the external device. The minimum time between exposure start and next exposure start is 25 µs (for full image).

Because the maximal frame rate is dependent on the read-out time of the digital array data, several array capture options are selectable for higher frame rates.

Image Size	Minimum exposure interval time in case of internal exposure generation (us)	Frame rate (frame/sec)
80x120	24.96	40064
80x60	12.96	77160
40x120	12.96	77160
40x60	6.96	143678
40x30	3.84	260416

Table 2: Frame rates for the supported image sizes

See configuration settings in the “Imager Control0” Register.

2.3.1 Exposure

For external exposure control a GPIO can be configured. For internal exposure control, a register can be set. There is a continuous mode where the exposure can be set via registers also the repeat time.

2.3.2 Pixel Data Read Out

The exposure signal can come from an external source or it can be generated internally.
Each TDC converts the image data to 8 bits, thus 640-bit or 320-bit incoming data arrives every 200ns or 100ns, respectively. This data is then multiplexed out on the 32-bit or 16-bit output pads every 10ns, on the rising edge of the 100MHz I/O clock.
Depending on the pixel accuracy, either 4 full pixels (4x8-bit) or 4 pixels with reduced accuracy (4x4-bit) are transferred on each I/O clock rising edge. In the latter case, only the 4 most significant bits of a pixel are used to save a total of 16 pins at the expense of lower pixel accuracy.

- 4 x 8-bit pixel mapping with full accuracy (readout_mode 0x0):
  mux0_data_o[7:0] = {$pixel_{4n+0}$[7:0]}
  mux1_data_o[7:0] = {$pixel_{4n+1}$[7:0]}
  mux2_data_o[7:0] = {$pixel_{4n+2}$[7:0]}
  mux3_data_o[7:0] = {$pixel_{4n+3}$[7:0]}

- 4 x 4-bit pixel mapping with reduced accuracy (readout_mode 0x1):
  mux0_data_o[7:0] = {$pixel_{2n+1}$[7:4], $pixel_{2n}$[7:4]}
  mux1_data_o[7:0] = {$pixel_{2n+3}$[7:4], $pixel_{2n+2}$[7:4]}

Throughout the data transfer, the datavalid signal is kept high, which can be used to sample the pixel data by the digital receiver on the rising edge of the IO clock. The length of the transfer depends on the image size because only the valid pixels are selected and transmitted from the middle of the image, yielding a higher frame rate for smaller images.

An optional framesync signal is also available through the GPIOs, which can be used for measurement purposes: two preamble pulses without data are followed by additional framesync pulses at the beginning of each transmitted line.

The timing diagrams below show the operation of the parallel interface for the biggest image (80x120) and the smallest image (40x30), respectively. Note that for smaller images, only the valid pixels are selected and transferred from the middle of the image, as indicated by the corresponding numbers in the diagrams. Both waveforms show the 4 x 8-bit mode. In the 4 x 4-bit reduced accuracy mode, the timing is identical except that only the two lower byte lanes are used with the pixel mapping described above.
The first data coming from the readout mux are always from the left top corner of the imager (exact coordinates are depending on the selected resolution – for all modes, the readout is centered to the center of the imager).

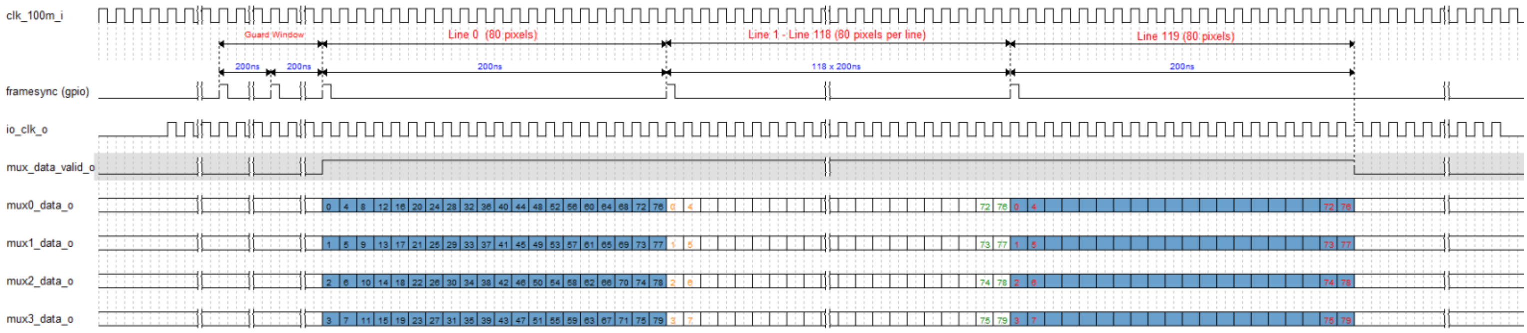


Figure 3: Readout Mux output timing for an 80x120 image

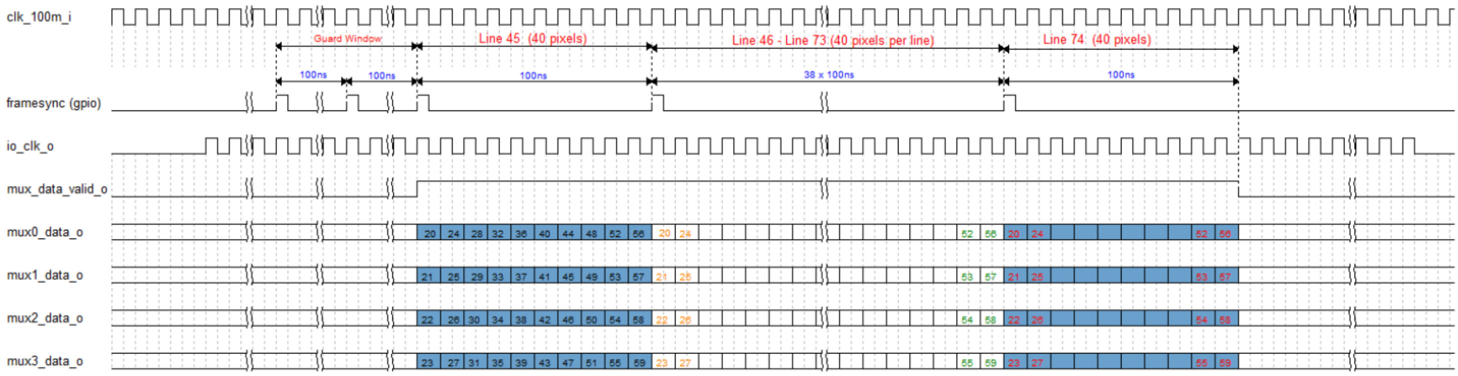


Figure 4: Readout Mux output timing for a 40x30 image

Note that one line can be read and transferred in 200ns if the image size is set to 80 pixels per line, whereas it only takes 100ns when an image size with 40 pixels per line is selected.

2.4 Power management

The chip is supplied with a 3.3V supply and a negative 1.5V supply (relative to Ground). The negative 1.5V supply powers only the Imager array (PPD's). The 3.3V main supply is feeding two 1.8V regulators supplying all internal blocks. For isolating the internal sensitive blocks, the output of the V1V8 regulator is external capacitive buffered and the filtered supply is feed back to the device using separate pins.
For the 32 high speed I/O's, a separate LDO is implemented to supply these drivers. For the generation of the negative 1.5V supply, an internal PWM regulated pulse generator is implemented (Pin CP_SW) to feed two external Schottky diodes and two capacitors. At the V1N5 PIN the negative voltage is inserted again, measured and regulated to -1.5V via internal PWM drive. The Charge Pump can be enabled via register set. The LED driver runs from his own supply and GND pins to minimize the coupling to the remaining functions.

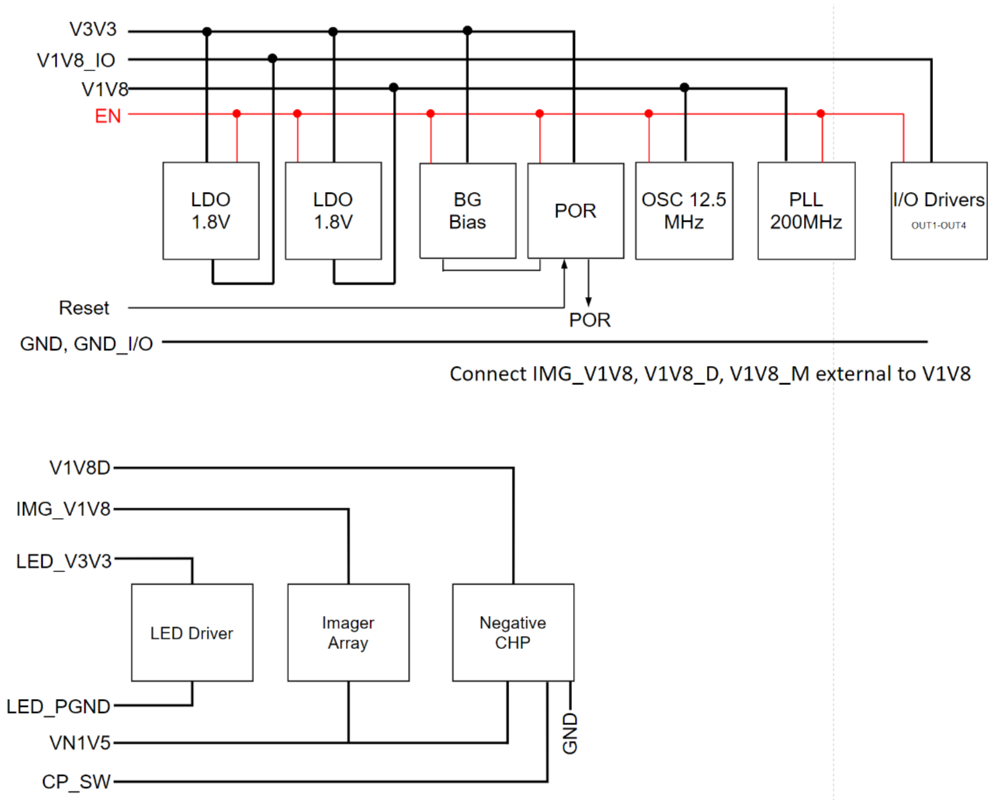


Figure 5: Power Management Diagram

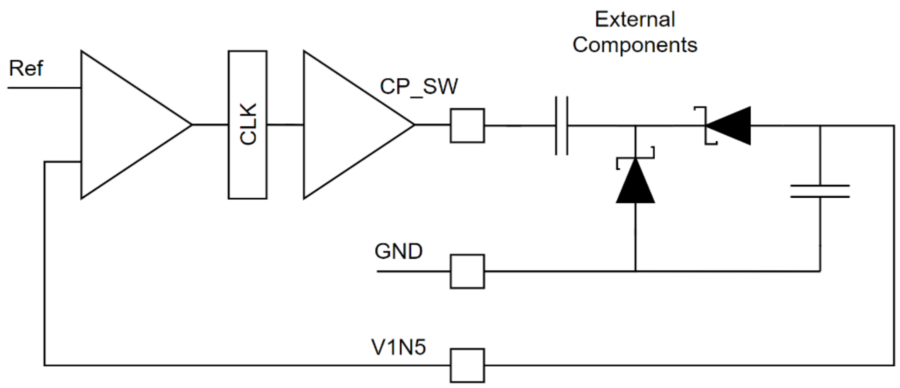


Figure 6: Negative Charge Pump V1N5V

2.5 LED Driver

An on-chip LED Driver with forward current up to 40mA is implemented to cover both Infrared IR, and Laser-diode light sources. The Forward-voltage of LED can be up to 2.4V. The Supply-Voltage for the single-LED is 3.3V and the Constant-Current drive required for driving can be set as 1mA to 40mA in steps of 2.5mA. Additionally, to the current setting, a PWM signal of up to 156 kHz can be used to dim the light.
The PWM signal can be fed via a configurable GPIO pin or the internal PWM generation can be used. Using a configurable GPIO pin the internal generated PWM signal can also be used to control an external LED driver.
For enabling and configuration, see LED Driver Register section.

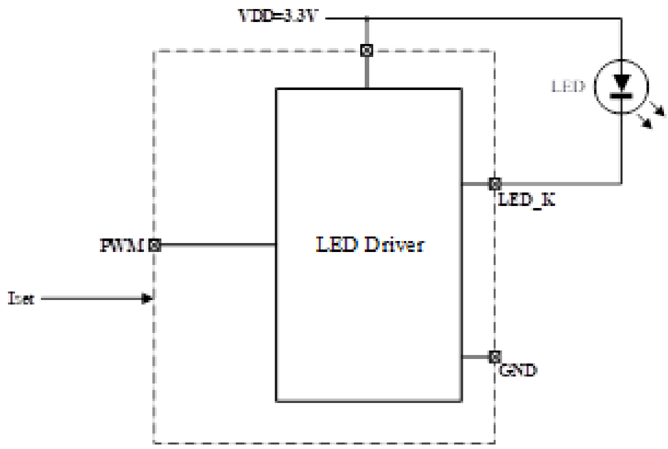


Figure 7: Simplified LED Driver block diagram

Programming settings to program the output current:

IPROG[7:0]	Drive Current (mA)
00000111	1.04
00001001	1.35
00001010	1.5
00001100	1.82
00001101	1.98
00001110	2.13
00001111	2.29
00010001	2.59
00100001	5
00110001	7.5
00110110	10
01010010	12.5

IPROG[7:0]	Drive Current (mA)
01100010	15
01110010	17.5
10000011	20
10010011	22.5
10100100	25
10110100	27.5
11000100	30
11010101	32.5
11100101	35
11110101	37.5
11111111	40

Table 3: IPROG settings to set the output current

The IPROG setting bits are located in the LED Driver register.

3 Register Bank

The Register Bank implements all the configuration registers. The registers are accessible externally via the SPI interface. The width of the address is 16 bits while the data is also 16 bits wide.

3.1 Register Map

Address	Name	Reset	Description
0x0	Revision	0xB20	Revision register.
0x2	Product ID	0x8020	Product identifier register.
0x6	Status	0x0	Status register to show the state of Boot Done.
0x8	GPIO Ctrl	0x0	Control register to select one of the GPIO functions when an MSIO is set to GPIO mode.
0x10	Imager Control	0x0	Control register for starting/stopping the imager in the selected mode.
0x12	Imager Config0	0x79	Configuration register for the imager (image size, exposure mode and power-on ramp-up time).
0x14	Imager Config1	0x1FA	Configuration register for the imager (exposure length).
0x16	Imager Config2	0x300F	Configuration register for the imager (continuous mode exposure time interval).
0x18	Imager Config3	0x0	Configuration register for the imager
0x20	LED Control	0x0	Led control register.
0x22	LED PWM	0x1C0A	Led PWM configuration register to define frequency and duty cycle for the generated PWM signal.
0x24	CP Config	0x0	Charge pump configuration register to define the CP_CLK clock frequency.
0x30	Imager Config4	0x71	Configuration register for the imager (power control for the analog array).
0x32	Image Count	0x0	Image counter status register. Shows the number of received images.
0x34	Image Count Threshold	0x0	Image counter threshold register to generate an interrupt when Image Count reaches this value.
0x36	Interrupt Enable	0x0	Interrupt enable register to mask the sources for the IRQ interrupt.
0x38	Raw Interrupt Status	0x0	Raw interrupt status. Shows the status of the interrupts before masking by the Interrupt Enable Register

Table 4: Register Map

3.1.1 Revision Register (0x0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Major Revision								Minor Revision							
RO								RO							

Figure 8: Revision Register

Bit	Type	Reset	Field	Description
15-8	RO	0x0B	Major Revision	Major revision.
7-0	RO	0x00	Minor Revision	Minor revision. Depending on the version, readout can be 0x20, 0x10 or 0x00.

Table 5: Revision Register Field Descriptions

3.1.2 Product ID register (0x2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fill bits				Product Identifier				Product Sub Family Identifier				Product Family Identifier			
RO				RO				RO				RO			

Figure 9: Product ID Register

Bit	Type	Reset	Field	Description
15-12	RO	0x8	Fill bits	Reads 0x8.
11-8	RO	0x0	Minor Revision	Reads 0x0 for the C110C product
7-4	RO	0x2	Product Sub-Family identifier	Reads 0x2 for the Cheetah Sub-Family (C110C sub-family)
3-0	RO	0x0	Product Family Identifier	Reads 0x0 for the C110 family

Table 6: Product ID Register Field Descriptions

3.1.3 Status Register (0x6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BootDone	Reserved														
RO	RO														

Figure 10: Status Register

Bit	Type	Field	Description
15	RO	Boot Done	Set to high when the boot sequence has been completed, all trim data is fetched from eFuse
14-0	RO	Reserved	Reserved, read returns 0

Table 7: Status Register Field Descriptions

3.1.4 GPIO Ctrl Register (0x8)

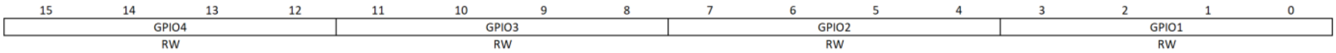


Figure 11: GPIO Ctrl Register

Bit	Type	Reset	Field	Description
15-12	RW	0x0	GPIO4	General purpose IO setting for the MSIO4 pin
11-8	RW	0x0	GPIO3	General purpose IO setting for the MSIO3 pin
7-4	RW	0x0	GPIO2	General purpose IO setting for the MSIO2 pin
3-0	RW	0x0	GPIO1	General purpose IO setting for the MSIO1 pin

Table 8: GPIO Ctrl Register Field Descriptions

This control register selects one of the GPIO functions.
The following table shows what GPIO functions can be selected for each port separately. Note that if the same input function is selected for more than one port, then these ports are OR-ed before reaching the internal digital logic.

	GPIO1<3:0> **GPIO1**	GPIO2<3:0> **GPIO2**	GPIO3<3:0> **GPIO3**	GPIO4<3:0> **GPIO4**
0	-	-	-	-
1	img_en_in	img_en_in	img_en_in	img_en_in
2	img_exposure_in	img_exposure_in	img_exposure_in	img_exposure_in
3	led_pwm_in	led_pwm_in	led_pwm_in	led_pwm_in
4	io_clk_out	io_clk_out	io_clk_out	io_clk_out
5	framesync_out	framesync_out	framesync_out	framesync_out
6	data_valid_out	data_valid_out	data_valid_out	data_valid_out
7	led_pwm_out	led_pwm_out	led_pwm_out	led_pwm_out
8	en_array_in	en_array_in	en_array_in	en_array_in
9	irq_out	irq_out	irq_out	irq_out

Table 9: GPIO configuration

NOTE1: The GPIOS have priority over the registers: GPIO always overrides a conflicting register setting. This is related to “img_en_in” and “img_exposure_in”.

NOTE2: To enable the external exposure mode, select the signal “img_exposure_in” on any of the GPIOs while also clearing the EXT_TRIG bit in the Imager Config0 Register. Alternatively, by setting EXT_TRIG bit to 1, this GPIO signal can be used as an external trigger pulse to start the internal exposure generation.

3.1.5 Imager Ctrl Register (0x10)

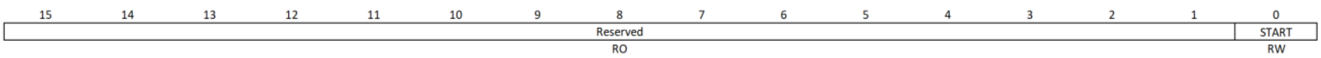


Figure 12: Imager Ctrl Register

Bit	Type	Reset	Field	Description
15-1	RW	0x0	Reserved	Reserved, read returns 0.
0	RW	0x0	START	Start bit for the internal exposure.

Table 10: Imager Ctrl Register Field Descriptions

If none of the GPIOs is set to “img_exposure_in”, then setting the Start bit from 0 to 1 will trigger the internal exposure generation. Depending on the EXP_MODE bit in the Imager Config0 Register, the internal exposure can run only once (single exposure mode) or continuously (continuous exposure mode). In continuous mode, the software must clear the Start bit to disable the exposure generation, which will cause the Cheetah hardware to stop after the ongoing exposure cycle has finished. The exposure length and exposure periodicity must be configured properly via the Imager Config1 Register and the Imager Config2 Register, respectively.
NOTE1: Irrespective of the exposure mode, the software must always finish the exposure sequence by clearing the Start bit as the new sequence is strictly triggered by a 0 to 1 transition.
NOTE2: If any of the GPIOs is set to “img_exposure_in”, then the START bit cannot start the exposure sequence. In this case, depending on the EXT_TRIG bit in the Imager Config0 Register, either an external exposure signal is applied or an external trigger pulse is used to start the exposure sequence. Even if started by an external trigger, the exposure can still be continuous if both the EXP_MODE bit in the Imager Config0 Register and the START bit are set to 1 before the external trigger pulse is generated.
NOTE3: Continuous exposure generation stops if either the EXP_MODE in the Imager Config0 Register or the START bit is cleared to 0.

3.1.6 Imager Config0 Register (0x12)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMG_AON		Reserved						EN_IMG_TH					EXT_TRIG	EXP_MODE	EN_IMG
RW		RO						RW					RW	RW	RW

Figure 13: Imager Config0 Register

Bit	Type	Reset	Field	Description
15	RW	0x0	IMG_AON	Imager Always On. If set to one, the imager is Always On when enabled by EN_IMG. If set to zero, the EN_IMG bit only enables the imager temporarily during active exposure and pixel processing.
14-12	RW	0x0	IMG_SIZE	Image Size. The full image size (default) is 80x120. Smaller images are created by capturing a rectangular area in the center of the full image. 0x0: 80x120 (full image) 0x1: 80x60 0x2: 40x120 0x3: 40x60 0x4: 40x30 0x5-0x7: Reserved (defaults to full image).
11-3	RW	0xF	EN_IMG_TH	Enable Imager Threshold. The imager is enabled this number of prescaled cycles earlier than the start of the exposure signal. The presale value is defined in the EXP_CONT_PRESCALE bit-field in the Imager Config2 Register. The timer’s reference clock is 12.5MHz.
2	RW	0x0	EXT_TRIG	External Trigger. If set to one, any GPIO configured as “img_exposure_in” is used as an external trigger to start the exposure sequence. The positive trigger pulse must be wider than 80ns. If set to zero, any GPIO configured as “img_exposure_in” is directly connected to the imager

				as the exposure source. If none of the GPIOs is configured as "img_exposure_in", then this EXT_TRIG bit has no effect.
1	RW	0x0	EXP_MODE	Exposure Mode. If set to one, the continuous exposure mode is active. If set to zero, the single exposure mode is active.
0	RW	0x1	EN_IMG	Enable Imager. This bit enables the imager support modules (particularly the 100MHz oscillator) when none of the GPIOs is configured as "img_en_in". The imager can be enabled permanently if IMG_AON is set to 1 or it can only be enabled during the active exposure phase if IMG_AON is set to 0. The automatic enable operation assumes that all the timers are configured properly. EN_IMG has no effect when the imager is controlled through the "img_en_in" GPIOs.

Table 11: Imager Config0 Register Field Descriptions

This configuration register defines the image size, selects the exposure mode and configures when and how the imager support modules should be enabled.
If any of the GPIOs is configured as "img_exposure_in", then this register defines if the external GPIO signal is merely a trigger to start the internal exposure generation or it must be treated as an external exposure signal, which is directly routed to the pixel controller bypassing the internal exposure generator.
If any of the GPIOs is configured as "img_en_in", then the imager support modules are directly enabled by that external GPIO signal overriding any other register setting. If no GPIO is configured as "img_en_in", then this register can be used to enable the imager support modules permanently or temporarily during active exposure and pixel processing. In the temporary case, this register also defines how much time the imager support modules need for ramping up before the actual exposure signal is generated.

3.1.7 Imager Config1 Register (0x14)

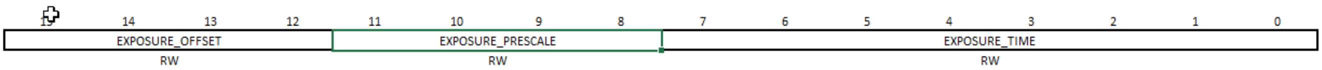


Figure 14: Imager Config1 Register

Bit	Type	Reset	Field	Description
15-12	RW	0x0	EXPOSURE_OFFSET	Exposure offset. Used in the exposure length timer and defines the number of fine-tune cycles, where the fine-tune cycle period is a quarter of the prescaled cycle period.
11-8	RW	0x1	EXPOSURE_PRESCALE	Clock pre-scaler down from 25MHz. Defines the division for the pre-scaled clock used in the exposure length timer. The pre-scaled clock frequency is 25MHz divided by [EXPOSURE_PRESCALE+1].
7-0	RW	0xFA	EXPOSURE_TIME	Exposure time. Used in the exposure length timer and defines the number of prescaled cycles.

Table 12: Imager Config1 Register Field Descriptions

This configuration register defines the length of the exposure and is used during internal exposure generation. The exposure length is given by the flowing formula, where $T_{CLK\_PRESCALE\ +\ 1}$ means the duration of one pre-scaled cycle.

Exposure time = EXPOSURE_OFFSET * [($T_{CLK\_PRESCALE+1}$) /4] + EXPOSURE_TIME * ($T_{CLK\_PRESCALE\ +\ 1}$)

3.1.8 Imager Config2 Register (0x16)

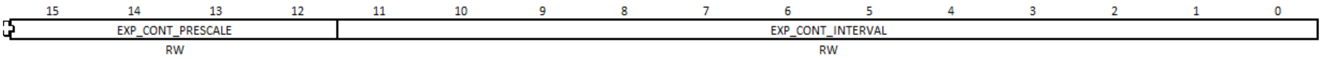


Figure 15: Imager Config2 Register

Bit	Type	Reset	Field	Description
15-12	RW	0x3	EXP_CONT_PRESCALE	Continuous exposure clock pre-scaler down from 4MHz. Defines the division for the prescaled clock used in the continuous exposure interval timer. The prescaled clock frequency is 4MHz divided by [EXP_CONT_PRESCALE+1].
11-0	RW	0xF	EXP_CONT_INTERVAL	Continuous exposure interval. Used for configuring the periodicity in continues exposure mode by defining the minimum number of prescaled cycles between two exposure rising edges.

Table 13: Imager Config2 Register Field Descriptions

This register configures the periodicity in continuous mode by defining the minimum time interval between two consecutive exposure starts.

Exposure interval = EXP_CONT_INTERVAL * ($T_{EXP\_CONT\_PRESCALE\ +\ 1}$)

3.1.9 Imager Config3 Register (0x16)

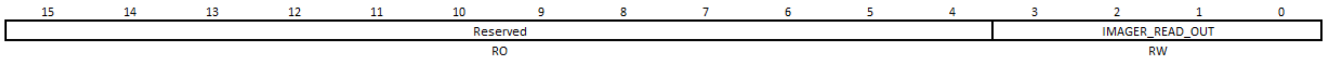


Figure 16: Imager Config3 Register

Bit	Type	Reset	Field	Description
15-3	RW	0x0	Reserved.	Reserved, read returns 0.
0	RW	0x0	PIXEL_ACC	Pixel Accuracy. Defines the number of pins for transferring pixel data through the parallel interface. 0x0: Full pixel accuracy with 4x8-bit pixel data. 0x1: Reduced pixel accuracy with 4x4-bit pixel data.

Table 14: Imager Config3 Register Field Descriptions

3.1.10 Led Control Register (0x20)

Figure 17: Led Driver Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						IPROG7	IPROG6	IPROG5	IPROG4	IPROG3	IPROG2	IPROG1	IPROG0	LED_AON	EN_LED
RO						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Type	Field	Description
15-10	RO	Reserved	Reserved, read returns 0
9	RW	IPROG7	IPROG7 – LED Driver output current.
8	RW	IPROG6	IPROG6 – LED Driver output current.
7	RW	IPROG5	IPROG5 – LED Driver output current.
6	RW	IPROG4	IPROG4 – LED Driver output current.
5	RW	IPROG3	IPROG3 – LED Driver output current.
4	RW	IPROG2	IPROG2 – LED Driver output current.
3	RW	IPROG1	IPROG1 – LED Driver output current.
2	RW	IPROG0	IPROG0 – LED Driver output current.
1	RW	LED_AON	LED driver Always On. If set to one, the LED driver is Always On when enabled by the EN_LED bit. If set to zero, the EN_LED bit only enables the LED driver temporarily during active exposure and pixel processing.
0	RW	EN_LED	Enables the Led Driver

Table 15: Led Driver Register Field Descriptions

This register sets the LED Driver output current and configures when the LED Driver is enabled. The LED Driver can be enabled permanently or temporarily during active exposure and pixel processing. In the temporary case, it is controlled in the same way as the imager, thus it is also enabled EN_IMG_TH time before the actual exposure signal is generated.
Note: The LED Driver is turned on by the led_en_o output signal. When the internally generated LED PWM signal is used, it is only active when led_en_o is also asserted.

3.1.11 LED PWM Register (0x22)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LED_CLK_PRESCALE						Reserved					LED_PWM				
RW						RO					RW				

Figure 18: LED PWM Register

Bit	Type	Reset	Field	Description
15-10	RW	0x7	LED_PWM_FREQ_DIV	LED PWM frequency divider down from 625kHz. The LED PWM frequency is 625kHz divided by [LED_PWM_FREQ_DIV+1].
9-5	RO	0x0	Reserved	Reserved, read returns 0.
0	RW	0xA	LED_PWM_DUTY	Sets the LED PWM duty cycle from 0% (no signal) to 100% (always on) in 5% steps. A value greater than 0x14 is also interpreted as 100%.

Table 16: Imager Config1 Register Field Descriptions

This register configures the frequency and duty cycle for the internally generated LED PWM signal.

3.1.12 CP Config Register (0x24)

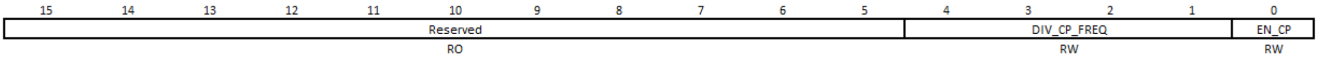


Figure 19: LED PWM Register

Bit	Type	Reset	Field	Description
15-5	RO	0x0	Reserved	Reserved, read returns 0.
4-1	RW	0x0	CP_FREQ_DIV	Charge pump frequency divider down from 1MHz. Defines the division for the CP_CLK signal. The charge pump frequency is 1MHz divided by [DIV_CP_FREQ+1].
0	RW	0x0	EN_CP	Enables the CP_CLK output.

Table 17: Imager Config1 Register Field Descriptions

This register activates the cp_clk_o output for the external charge pump and configures its frequency.

3.1.13 Imager Config4 Register (0x30)

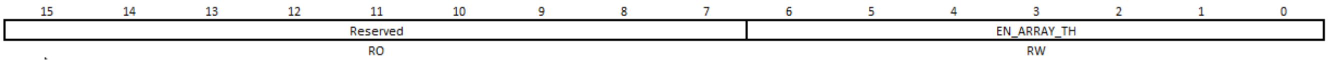


Figure 20: Imager Config4 Register

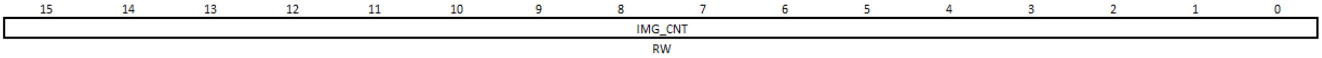
Bit	Type	Reset	Field	Description
15-9	RO	0x0	Reserved	Reserved, read returns 0.
8-2	RW	0x1C	EN_ARRAY_TH	Threshold time to enable the analog array. The respective analog blocks must be enabled this period of threshold time before the exposure ends. This time is only applicable in automatic mode, when ARRAY_AON is set to zero. The time unit is **us.**
1	RW	0x0	ARRAY_AON	Analog Array Always On. If set to one, the analog array is Always On when enabled by the EN_ARRAY bit. If set to zero, the EN_ARRAY bit enables the automatic power control of the analog array, which is then dynamically turned on when the imager is active.
0	RW	0x1	EN_ARRAY	Enables the analog array.

Table 18: Imager Config4 Register

This register configures when and how the analog array is enabled. The respective analog blocks can be turned on permanently or only temporarily during active exposure and image processing.
If automatic power control is selected (ARRAY_AON=0, EN_ARRAY=1), the analog array is enabled EN_ARRAY_TH time before the exposure ends. It is then disabled at the end of the image sequence in single mode or stays on in continuous mode.
Note: The Analog array is turned on by the en_array_o output signal.

3.1.14 Image Count Register (0x32)

Figure 21: Imager Count Register



Bit	Type	Reset	Field	Description
15-0	RW	0x0	IMG_CNT	Image Count. Counts the number of images starting from zero until it reaches the threshold value defined in the Image Count Threshold Register. The counter can be restarted by writing 0x0 to it.

Table 19: Image Count Register Field Descriptions

This register implements an image counter, which is incremented at the end of each image sequence until it reaches the threshold value defined in the Image Count Threshold Register. In order to re-activate the counter, the software must reset it to 0x0. Upon reaching the threshold value, an interrupt is also generated if the respective configuration bits are set properly.

3.1.15 Image Count Threshold Register (0x34)

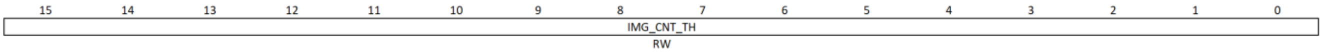


Figure 22: Image Count Threshold Register

Bit	Type	Reset	Field	Description
15-0	RW	0x0	IMG_CNT_TH	Image Count Threshold. If the image counter reaches this threshold value, it stops and a raw interrupt is also generated. The counter can be restarted by writing 0x0 to it.

Table 20: Image Count Threshold Register Field Descriptions

This register defines the image count threshold, which is the maximum value the image counter can reach before it stops. When the image counter reaches this threshold value, it sets the IMG_DONE status bit in the Raw Interrupt Status Register and generates an interrupt if the corresponding interrupt source is enabled and one of the GPIOs is configured as “irq_out”.

3.1.16 Interrupt Enable Register (0x36)

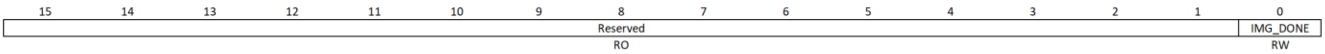


Figure 23: Interrupt Enable Register

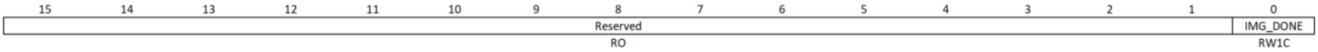
Bit	Type	Reset	Field	Description
15-1	RO	0x0	Reserved	Reserved, read returns 0.
0	RW	0x0	IMG_DONE	Enables the IMG_DONE interrupt source. If set to one, the image counter generates an interrupt upon reaching the IMG_CNT_TH threshold value.

Table 21: Interrupt Enable Register Field Descriptions

This register enables or masks interrupts from being triggered on the IRQ pin. The enable bit is named after the respective interrupt source. In Cheetah, the only interrupt source is IMG_DONE, which is generated when the image counter reaches the IMG_CNT_TH threshold value. Setting the respective enable bit to one enables the interrupt triggering on the IRQ pin.
Note: IRQ is mapped onto the GPIO ports. Therefore, if interrupt is used, one of the GPIOs must be configured as “irq_out”.

3.1.17 Raw Interrupt Status Register (0x38)

Figure 24: Raw Interrupt Status Register



Bit	Type	Reset	Field	Description
15-1	RO	0x0	Reserved	Reserved, read returns 0.
0	RW1C	0x0	IMG_DONE	Interrupt status bit indicating that the hardware has finished capturing and processing a predefined number of images. The status bit is set to one when the image counter reaches the IMG_CNT_TH threshold value. Cleared by writing one to this bit field.

Table 22: Raw Interrupt Status Register Field Descriptions

This register shows the status of the interrupts before masking by the Interrupt Enable Register. In Cheetah, the only interrupt status bit is IMG_DONE, which is set to one when the image counter reaches the IMG_CNT_TH threshold value. If this interrupt is enabled, then the value of this status bit also appears on the IRQ pin. Writing one to this bit-field clears this status bit.
Note: IRQ is mapped onto the GPIO ports. Therefore, if interrupt is used, one of the GPIOs must be configured as “irq_out”.

4 SPI Slave

The purpose of the SPI slave module is to implement register accesses according to the commands sent by the external SPI master.

4.1 Overview

The module supports single access for the configuration registers.
A single access is implemented through the following sequence:

1. 8-bit command (single write or single read)
2. 16-bit address (configuration register address)
3. 16-bit data (configuration register data)

4.2 SPI Commands for accessing Registers

The Register access SPI commands are listed in the following sections and grouped according to the operational speed it can support. Each register access SPI command has 1-byte header, followed by 2-bytes of address and 2-bytes of data.
Depending on the used command, the SPI can work in two speed modes, as described below.

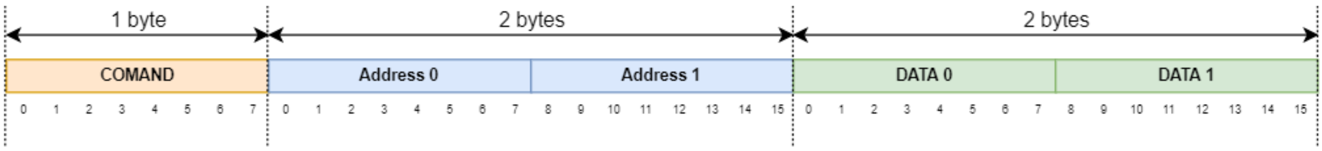


Figure 25: SPI Register Command

4.2.1 Slow SPI

The SPI Register access commands listed in Table 22 support SPI clock seed up to 3.125 MHz.

Command	Type	Endianness
0x30	READ	Big Endian
0x20	READ	Little Endian

Table 23: Slow SPI Register Access Commands

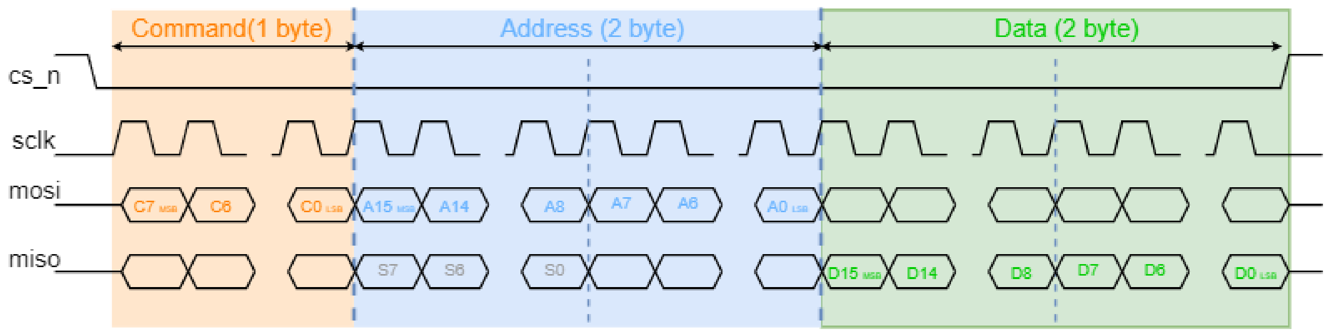


Figure 26: Slow SPI Register Read with Little Endian

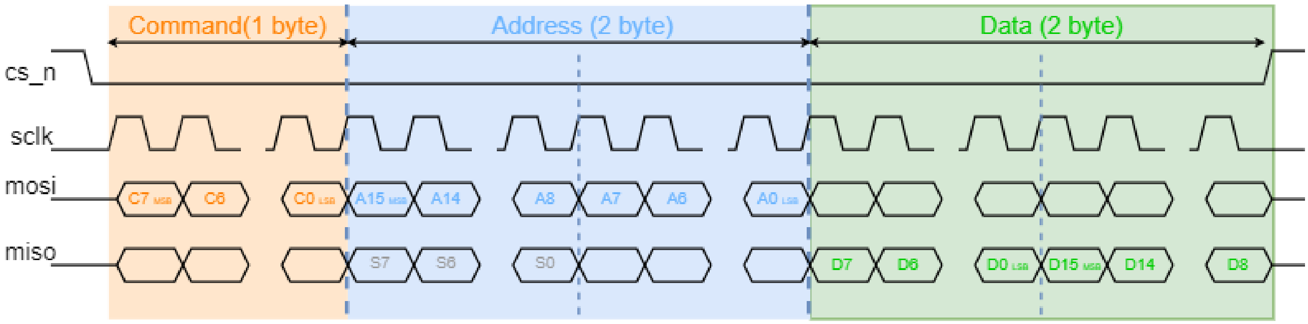


Figure 27: Slow SPI Register Read with Big Endian

4.2.2 Fast SPI

The SPI commands listed support SPI clock seed up to 15.625 MHz.

Command	Type	Endianness
0x32	READ	Big Endian
0x40	READ	Little Endian
0x36	WRITE	Big Endian
0x24	WRITE	Little Endian

Table 24: Fast SPI Register Access Commands

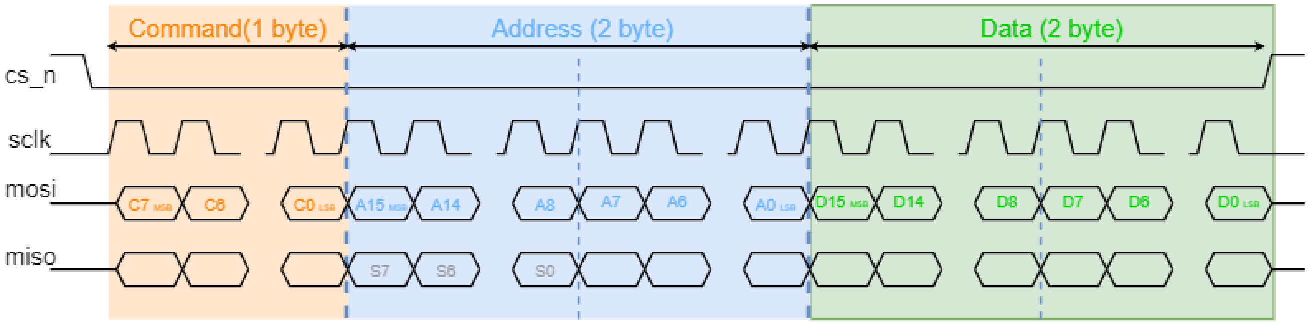


Figure 28: Fast SPI Register Write with Little Endian

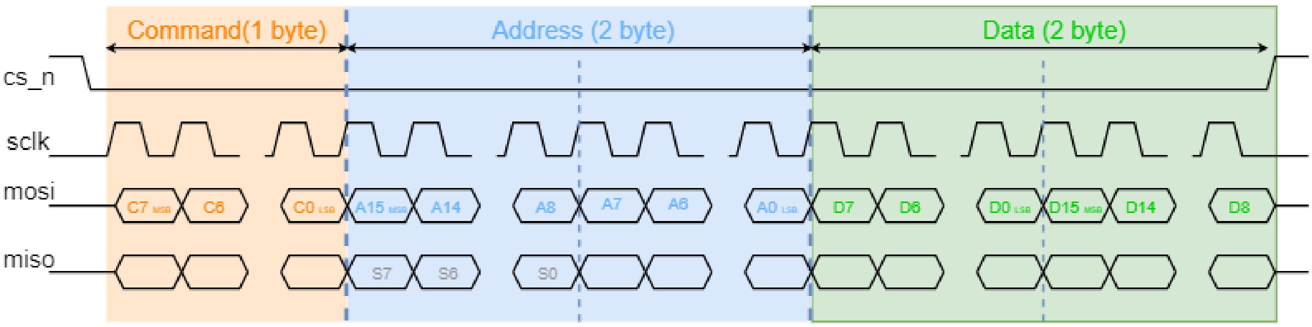


Figure 29: Fast SPI Register Write with Big Endian

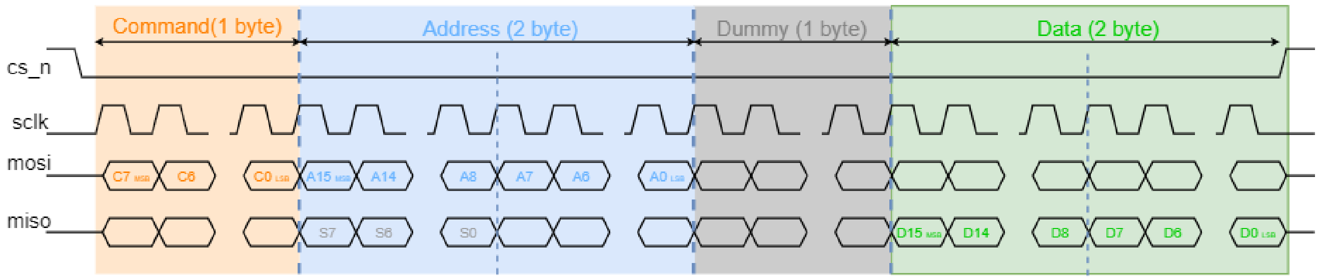


Figure 30: Fast SPI Register Read with Little Endian

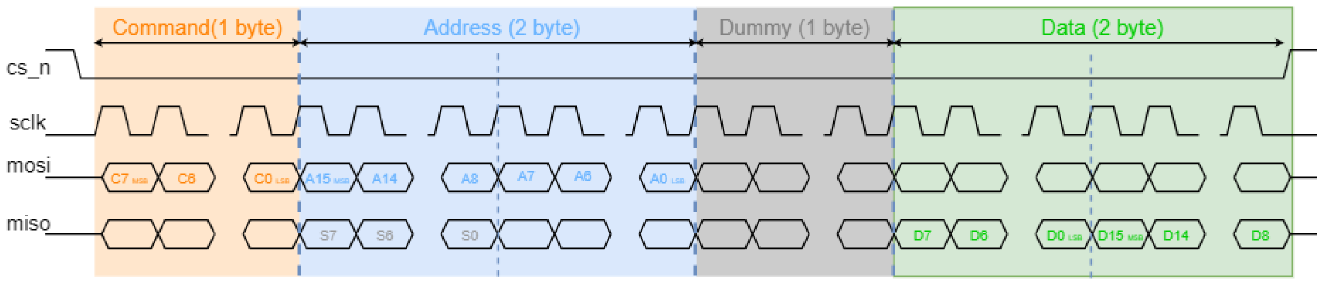


Figure 31: Fast SPI Register Read with Big Endian

<u>Note that when using the fast READ commands, the first byte of the return data is a dummy byte which needs to be discarded.</u>

4.3 Control Timing

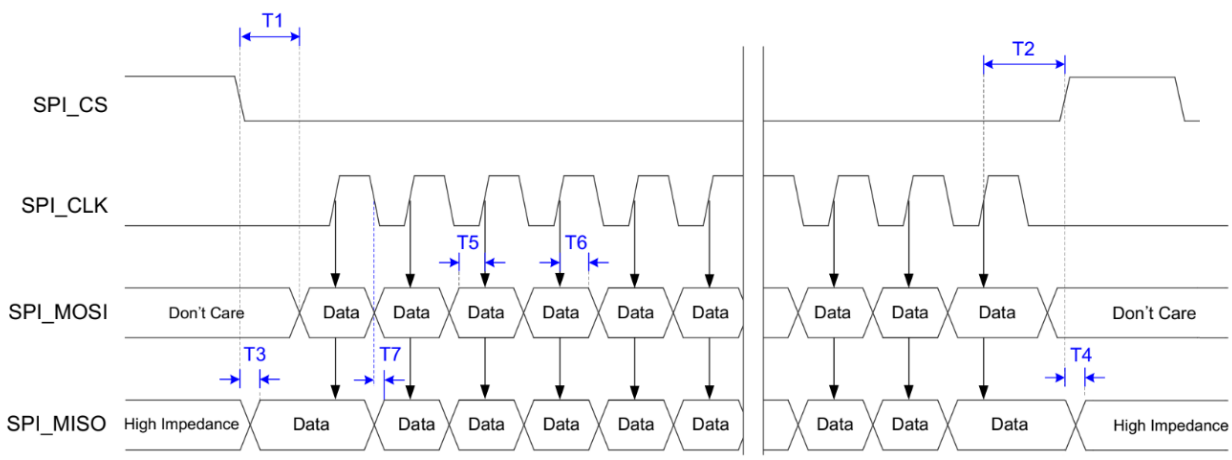


Figure 32: SPI Control Timing (Only Mode 0 supported)

Note: Timing related specifications can be found in the Electrical Characteristics for the SPI.

5 Absolute Maximum Ratings

Table 25: Absolute Maximum Ratings

ID	Pin	min	max	Unit	Condition
5.1	V3V3, LED_K, LED_V3V3	-0.5	4.3	V	
5.2	DATA_VAL, FRAMESYNC, CLK_IO, V1V8_IO, OUTx_x, IMG_V1V8, V1V8_D, V1V8, RES, ENABLE, SPI_CLK, SPI_MOSI, SPI_MISO, SPI_NCS, LED_PWM, V1V8_M	-0.5	2.2	V	
5.3	VN1V5	-2.2	0.5	V	

6 Range of functionality

6.1 ESD Robustness

Table 26: ESD Robustness

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
6.1.1	All pins	V_{esd}		-2	2	kV	HBM

6.2 Temperature, Thermal and Power

Table 27: Temperature, Thermal and Power

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
6.2.1	Storage temperature	$T_{Storage}$		-40	135	°C	
6.2.2	Storage time	$t_{Storage}$			10	year	
6.2.3	Maximum soldering temperature	T_{solder}			260	°C	For 40s (required for lead free soldering)
6.2.4	Operating ambient temperature	T_a		0	80	°C	

6.3 Active Supply Currents

Table 28: Active Supply Currents

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
6.3.1	Active current at V3V3 pin	I_{v3v3_on}	550			µA	Device enabled, Imager turned off
6.3.2	Off current at V3V3 pin	I_{v3v3_off}	100			nA	Device disabled, non-IR version
6.3.3	Active current at V3V3 pin	$I_{v3v3\_exp\_100}$	700			µA	Device enabled, Imager turned on, 100 fps
6.3.4	Active current at V3V3 pin	$I_{v3v3\_exp\_40k}$	30			mA	Device enabled, Imager turned on, 40 kfps, full resolution

6.4 Digital I/O

Table 29: Digital I/O

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
6.4.1	Digital I/O supply	V1V8	1.8	1.71	1.89	V	
6.4.2	Logic input low	V_{IL}		-0.3	0.3* VDDIO	V	
6.4.3	Logic input high	V_{IH}		0.7* VDDIO	VDDIO +0.3	V	
6.4.4	Logic input hysteresis	V_{IHYST}	80	30	150	mV	
6.4.5	Internal pull-down resistor for logic inputs	R_{PD}	30	10	50	kΩ	**PIN:** RES, ENABLE, SPI_CLK, SPI_MOSI, LED_PWM, GPIOx
6.4.6	Internal pull-up resistor for logic inputs	R_{PU}	30	10	50	kΩ	**PIN:** SPI_NCS
6.4.7	Logic output low	V_{OL}		0	0.3* VDDIO	V	0mA < I < 1mA
6.4.8	Logic output high	V_{OH}		0.7* VDDIO	VDDIO +0.3	V	0mA < I < 1mA

7 Electrical Characteristics

7.1 Power Supply – Main 1.8V Regulator

Table 30: EC table V1V8

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.1.1	V3V3 Power supply input	V3V3	3.3	2.97	3.63	V	
7.1.2	Output voltage	V_{OUT}	1.8	1.76	1.86	V	
7.1.3	Output current	I_{OUT}		35		mA	
7.1.4	External capacitor	C_{EXT}	2.2	1	10	µF	
7.1.5	Start-up time	t_{Start}			195	µs	

7.2 Power Supply – High Speed I/O 1.8V Regulator

Table 31: EC table V1V8 IO

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.2.1	V3V3 Power supply input	V3V3	3.3	2.97	3.63	V	
7.2.2	Output voltage	V_{OUT}	1.8	1.76	1.86	V	
7.2.3	Output current	I_{OUT}		100		mA	
7.2.4	External capacitor	C_{EXT}	2.2	1	10	µF	
7.2.5	Start-up time	t_{Start}	41			µs	

7.3 V3V3 Monitor

Table 32: EC table V3V3 Monitor

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.7.1	V3V3 Power supply input	V3V3	3.3	2.97	3.63	V	
7.7.2	Threshold LO-HI	VTHLH	2.29	1.90	2.62	V	
7.7.3	Threshold HI-LO	VTHHL	2.22	1.84	2.49	V	

7.4 LED Driver

Table 33: EC table LED Driver

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.4.1	Supply, Power-part of LED Driver	$V_{SUP\_LED\_POW}$	3.3	2.97	3.63	V	
7.4.2	Supply, Bias-part of LED Driver	$V_{SUP\_LED\_BIAS}$	1.8	1.71	1.89	V	
7.4.3	Output current accuracy	I_{acc}		-15%	+15%	mA	
7.4.4	Frequency Of Switching	Freq		9.765	625	kHz	
7.4.5	Output Current Settling time	T_{settle}			1.5	µs	Stand-by to Active
7.4.6	Output Current from Start	T_{enable}			5	µs	Power-down to Active

7.5 High Speed I/O

Table 34: EC table HS I/O

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.5.1	HS I/O supply	V1V8	1.8	1.71	1.89	V	
7.5.2	Clock input frequency	f_{out}	100			MHz	
7.5.3	Duty Cycle clock output	Duty_cycle	50			%	
7.5.4	Logic output low	V_{OL}		0	0.3* V1V8	V	0mA < I < 1mA No termination resistor
7.5.5	Logic output high	V_{OH}		0.7* V1V8	V1V8 +0.3	V	0mA < I < 1mA No termination resistor

Note: Pins OUTx_x

7.6 PLL

Table 35: EC table PLL

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.6.1	V1V8 supply	V1V8	1.8	1.71	1.89	V	
7.6.2	Frequency of output	f_{out}	100	98	102	MHz	CLK_IO pin frequency

7.7 POR

Table 36: EC table POR

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.7.1	V3V3 Power supply input	V3V3	3.3	2.97	3.63	V	
7.7.2	Threshold LO-HI	V_{tlh}	1.35	1.1	1.63	V	
7.7.3	Threshold HI-LO	V_{thl}	1.32	1.05	1.6	V	
7.7.4	Hysteresis	V_{hyst}	26	15	46	mV	

7.8 SPI

Table 37: EC table SPI

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.8.1	V1V8 supply	V1V8	1.8	1.71	1.89	V	
7.8.2	SPI_CLK frequency for legacy (slow) commands (Note 1)	F_{SPI}			3.125	MHz	See timing diagram in SPI Slave section
7.8.3	SPI_CLK period for legacy (slow) commands (Note 1)	T_{SPI}		320		ns	
7.8.4	SPI_CLK frequency for fast commands (Note 2)	F_{SPI}			15.62	MHz	
7.8.5	SPI_CLK period for fast commands (Note 2)	T_{SPI}		64		ns	
7.8.6	SPI_CLK duty cycle	Duty Cycle	50	40	60	%	
7.8.7	SPI_NCS Setup Time	T1		10		ns	
7.8.8	SPI_NCS Hold Time	T2		1		TSPI	
7.8.9	From SPI_NCS falling to SPI_MISO enable (Note 3)	T3			30	ns	
7.8.10	From SPI_NCS rising to SPI_MISO disable (Note 3)	T4			30	ns	
7.8.11	SPI_MOSI setup time	T5		10		ns	
7.8.12	SPI_MOSI hold time	T6		10		ns	
7.8.13	SPI_MISO delay time (Note 3)	T7			12	ns	

Note 1: If legacy (slow) SPI commands are used, then there is no dummy read data byte.
Note 2: If fast SPI commands are used, then the first read data byte must be discarded.
Note 3: Assume 80pF loading at SPI_MISO pin.

7.9 High Speed Imager

Table 38: EC table High Speed Imager

ID	Parameter	Symbol	Typical	min	max	Unit	Condition
7.9.1	V3V3 Power supply input	V3V3	3.3	2.97	3.63	V	
7.9.2	V1V8_D Digital supply input	V1V8_D	1.8	1.71	1.89	V	
7.9.3	IMG_V1V8 Imager supply input	IMG_V1V8	1.8	1.71	1.89	V	
7.9.4	VN1V5 Negative supply input	VN1V5	-1.5	-1.58	-1.43	V	
7.9.5	Pixel, Full Well	Q_{sat}	400			ke-	Information only
7.9.6	TDC, Number of bits	B_{tdc}	8	4	8	bits	
7.9.7	Effective number of bits	ENOB	5			bits	
7.9.8	Resolution	R_{es}	80 x 120			pixels	Information only
7.9.9	Imager size	I_{size}	1600 x 2400			um	Information only
7.8.10	Pixel size	P_{size}	20x20			um	Information only
7.9.11	Aspect ratio	R_{es}	1.5			#	Information only
7.9.12	Max frame rate	FR_{max}	40		260	kfps	Information only, depending on the selected resolution

8 Typical Application

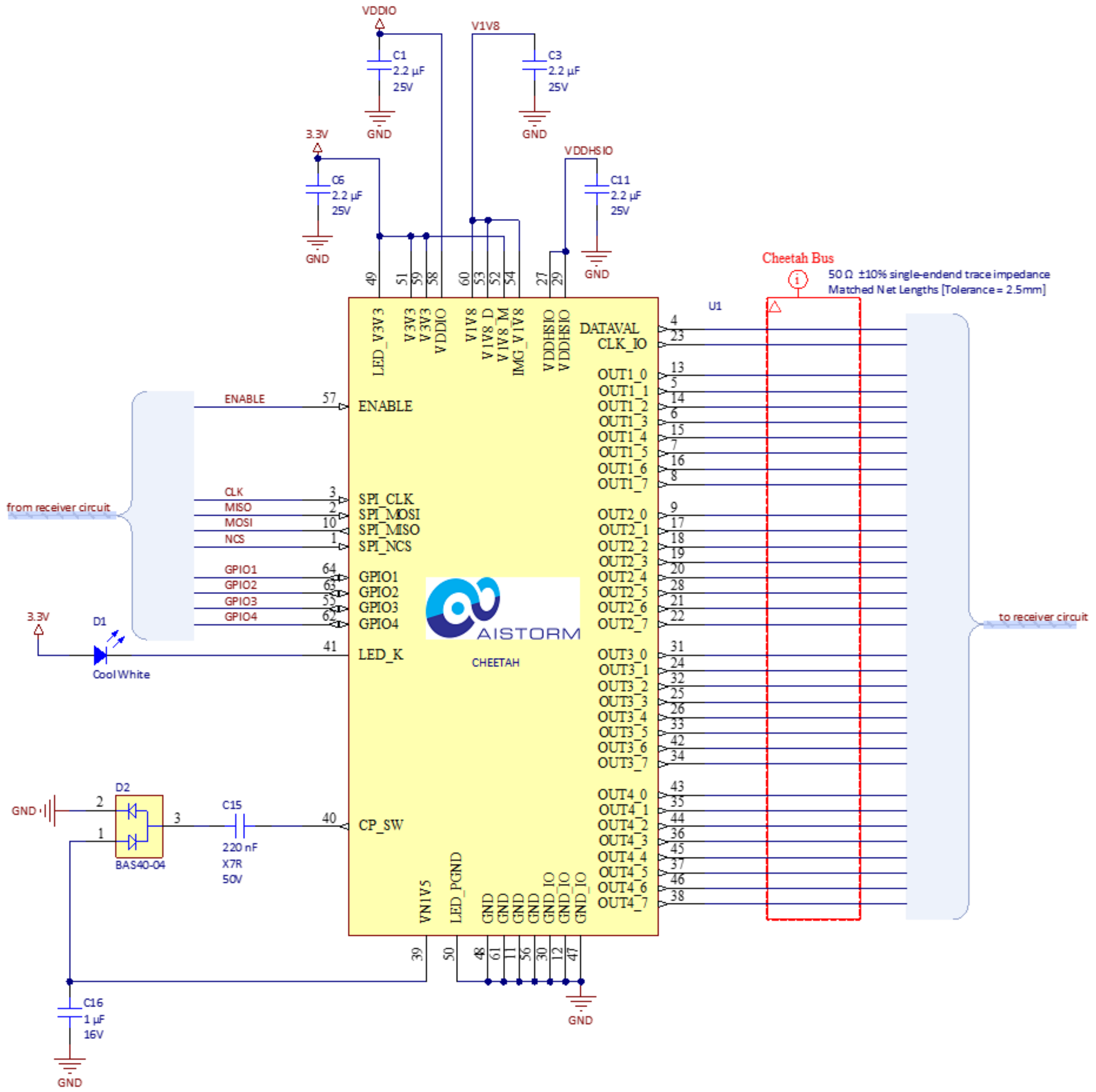


Figure 50: Typical Application

9 Board Layout Considerations

For both integrated LDOs it is recommended to use 2.2 µF capacitors for stability, placing these capacitors as close as possible to the LDO output pins.

The integrated charge pump for the negative supply requires a 220 nF pump capacitor, a 1 µF storage capacitor, and a dual Schottky diode with a very low forward voltage. The diode forward voltage reduces the efficiency of the charge pump, one recommended diode is the BAS40-04.

9.1 Power Supply

The power supply decoupling capacitors should be placed as close as possible to the power supply pins. A good approach is to place the decoupling capacitors as a first step when starting with the layout of the PCB and as a second step route the high-speed signals.

9.2 High-Speed output lines

The high-speed output lines should be routed above a solid ground layer as the reference plane. The ground plane should be connected to the GND_IO pins, with multiple vias to reduce the inductance. A high-speed signal line should be routed on a single layer, when possible, without any layer changes. When a layer change is necessary add close to the signal vias ground transfer vias connecting the adjacent ground planes together.

10 Package Information

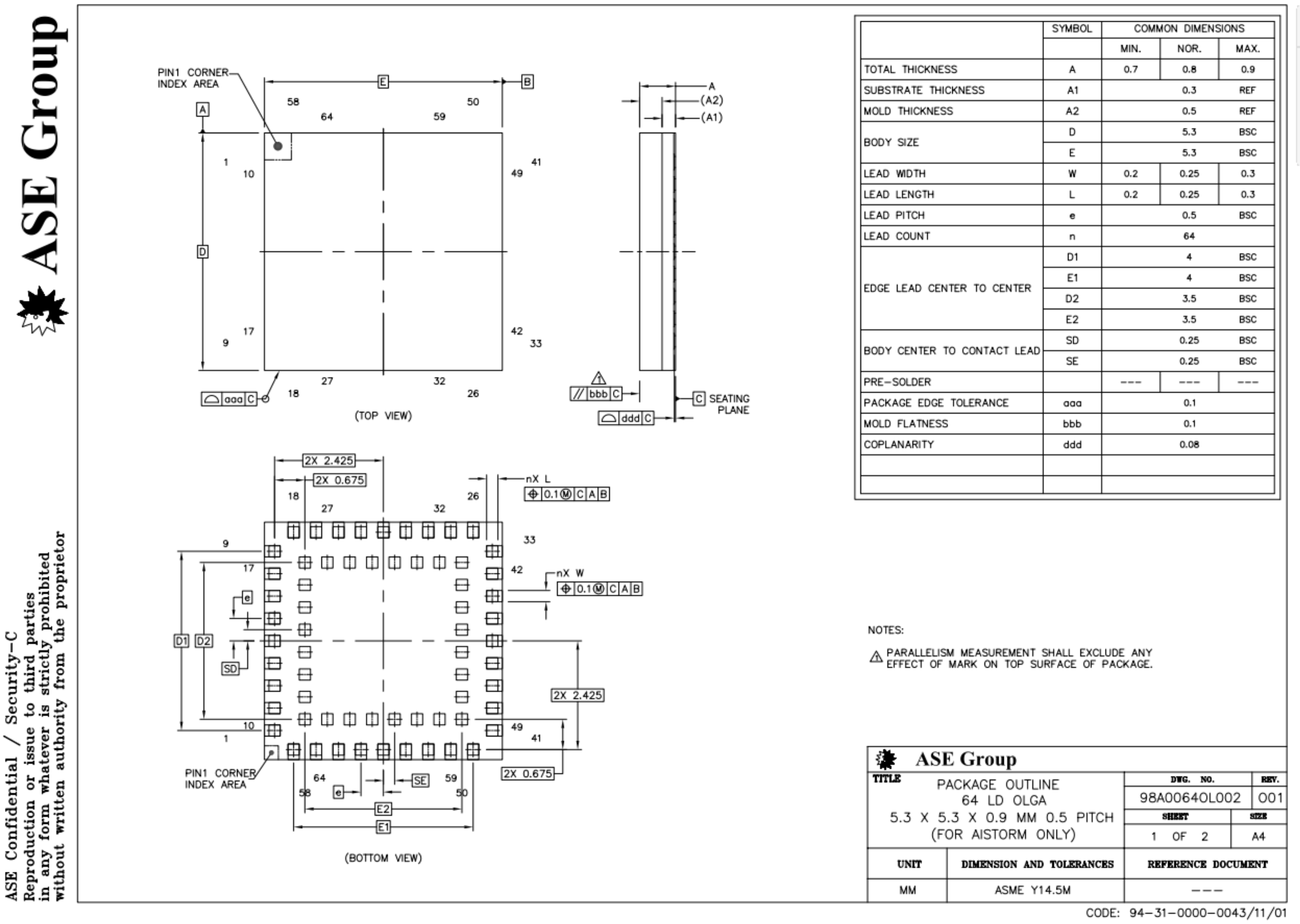


Figure 33: Package Information OLGA64 Package

11 Tape and Reel Information

Table 39: Tape and Reel Information

Package Type	# of Leads	Nominal Package Size	Pocket Tape		Pin 1 Orientation	Reel Size (mm)	Reel Size (inch)	Qantity per Reel
			Width	Pitch(P1)				
LGA	64	5.3x5.3x0.8mm	12mm	8mm	Top-Left	330mm	13"	TBD

12 Ordering Information

13 List of Abbreviations

Table 40: List of Abbreviations

Name	Description
HBM	Human Body Model
HS	High Speed
I/O	Input-Output
MSIO	Mixed Signal I/O
POR	Power-on reset
SPI	Serial Peripheral Interface
TBA	To Be Added
TBD	To Be Defined
TDC	Time to Digital Converter

14 Revision History

Table 41: Revision History

Revision	Date	Description	Author
0.1	2023-07-11	Initial revision	Erik Sibrai
0.2	2025-03-19	Format adjustments and minor corrections	Maximilian Heindel
1.0	2025-04-29	Document release	Maximilian Heindel

15 Errata List

Table 42: Errata List

Errata Number	Description
1	Using a horizontal resolution of 80 pixels, the first row does not work and should be dismissed.
2	The first captured picture is brighter than the following ones, if the time between the exposure starts is greater than 400 us.
3	If a pixel is in overflow (>254 dec.) the pixel below (in the next row) will show a value of 32 dec.

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