AIS2001 Analog Microphone Interface with Feature Extraction

General description

The AIS2001 “Monarch” is a smart analog MEMS microphone interface with included feature extraction. Ultra-low "always on" power consumption of < 250 µW. With proper dataset training accuracy levels greater than 95% are possible for speech and anomaly detection.

The proprietary charge domain feature extraction engine eliminates the need for data conversion and complex power-hungry DSP while generating the appropriate form of spectrogram for neural network word and sound classification input. This results in superior ultra-low power performance with no compromise in accuracy.

The analog front-end amplifier interfaces directly to single-ended analog MEMS microphones with minimum additional components. This allows for a significant power benefit compared to digital microphones. The AIS2001 can be easily interfaced to various other types of sensors such as accelerometers and heart rate monitors thanks to the variable gain input amplifier with high input impedance.

The AIS2001 development environment supports standard flows such as TensorFlow lite. The trained and quantized parameters can be stored directly in the on-chip SRAM. This provides ultimate flexibility for ultra-low power standalone applications.

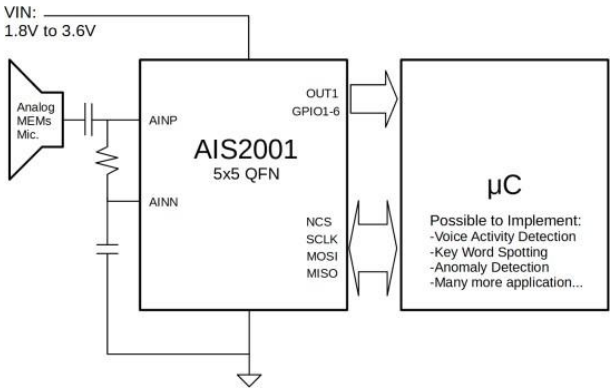
Features

- Low active power consumption of < 250 µW average power when running full Analog Signal Conditioning and Feature Extraction.
- Supports 32 frequency bins in Feature Extraction image.
- Allows for use of preset coefficients in ROM or for custom coefficients to be loaded into SRAM.
- Directly interfaces to analog MEMS microphone.
- SPI Interface (load coefficients, read audio and flags)
- On board ultra-low power regulator and clock.
- Supply operating range supports common analog MEMS microphone ranges.
  - VIN: 1.5V to 3.6V
  - AVDD: 1.2V
  - DVDD: 0.9V to 1.2V
- Direct powering of 1.2V regulated pins is supported for lowest power requirements.
- Small footprint in a 32 pin 5x5 QFN package.

Applications

- Wake-word recognition
- Acoustic Anomaly/Event Detection
- Event Based classifier templates

Typical Circuit



Example PSD Output

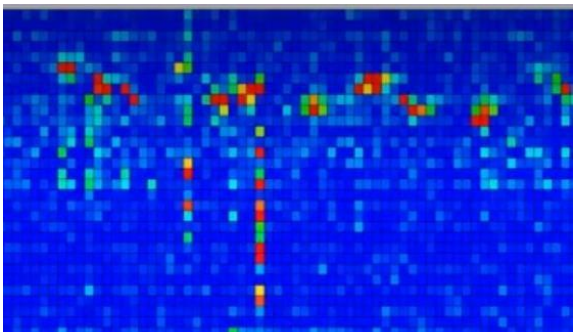


Table of Contents

1 Pin Description

Table 1: Pin Description

Pin number	Pin name	Type	Description
1	NC	-	Not connected
2	AGND	GND	Analog ground
3	AGND	GND	Analog ground
4	AGND	GND	Analog ground
5	AINN	IN	Inverting input of the input audio amplifier
6	IOPL	OUT	Analog output of the input audio amplifier
7	AINP	IN	Non-inverting input of the input audio amplifier
8	GPIO1	IN/OUT	General purpose input/output
9	NC	-	Not connected
10	IOPR	OUT	Analog output of the input audio amplifier
11	GPIO2	IN/OUT	General purpose input/output
12	GPIO3	IN/OUT	General purpose input/output
13	GPIO4	IN/OUT	General purpose input/output
14	OUT1	OUT	General purpose output
15	GPIO5	IN/OUT	General purpose input/output
16	GPIO6	IN/OUT	General purpose input/output
17	NC	-	Not connected
18	SCLK	IN	SPI clock input
19	NC	-	Not connected
20	MOSI	IN	SPI MOSI
21	NC	-	Not connected
22	MISO	OUT	SPI MISO
23	NC	-	Not connected
24	NCS	IN	SPI chip-select not
25	DGND	GND	Digital ground pin
26	DVDD	OUT	AIS2001 generated digital supply voltage
27	DVDD	OUT	AIS2001 generated digital supply voltage
28	DVDD	OUT	AIS2001 generated digital supply voltage
29	VIN	SUPPLY	Input voltage to the AIS2001
30	VIN	SUPPLY	Input voltage to the AIS2001
31	AVDD	OUT	AIS2001 generated analog supply voltage
32	AVDD	OUT	AIS2001 generated analog supply voltage
33	Exposed Pad	-	Not connected

Package Pinout

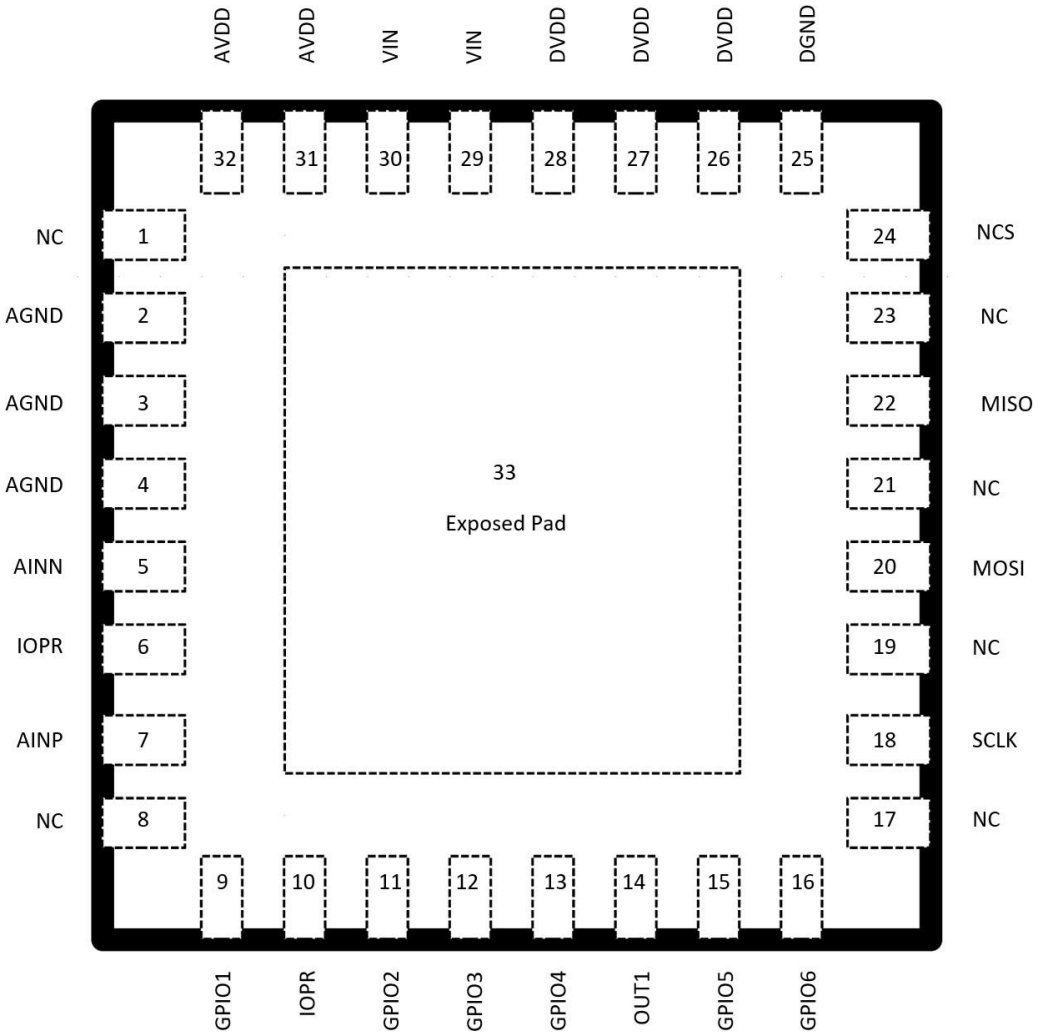


Figure 1: AIS2001 package pinout (top view)

2 Block Diagram

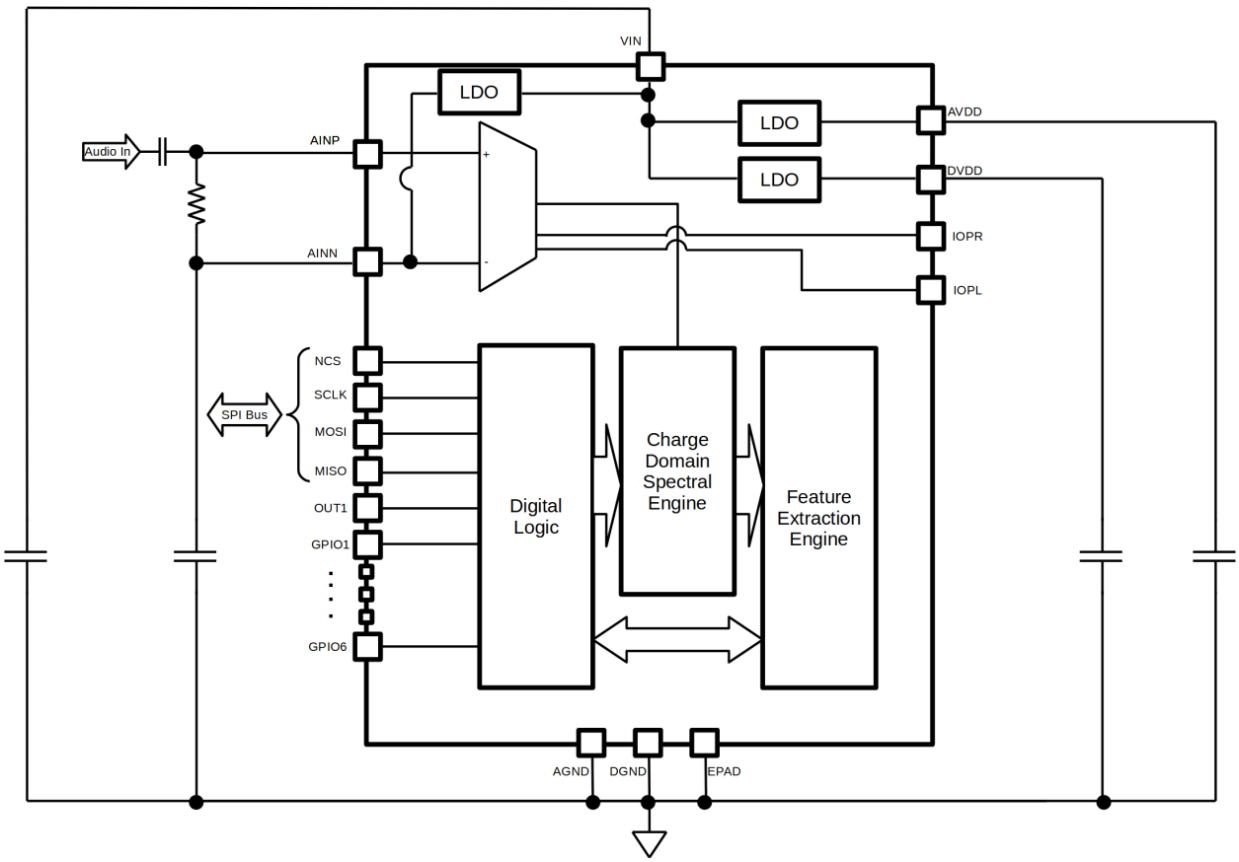


Figure 2: Block diagram

3 Register Bank

The Register Bank implements all the configuration registers. The registers are accessible externally via the SPI interface.

3.1 Overview

Part of the registers are 16 bits wide and can be accessed directly, others are 32 bits wide and are accessed indirectly.

3.1.1 Direct Registers

Table 2: Direct Registers

Address	Name	Type	Reset	Description
0x00	IWA	RW	0x0000	Address for an indirect register write
0x02	IWDH	RW	0x0000	Bits <31:16> of data for indirect register write
0x04	IWDL	RW	0x0000	Bits <15:0> of data for indirect register write
0x06	IWT	RW	0x0080	Indirect write configuration
0x08	IRA	RW	0x0000	Address for an indirect register read
0x0A	IRT	RW	0x0080	Indirect read configuration
0x0C	IRDH	RW	0x0000	Bits <31:16> of data for indirect register read
0x0E	IRDL	RW	0x0000	Bits <15:0> of data for indirect register read
0x10	ERST	RW	0x0000	System error capture
0x12	ERSA	RW	0x0000	Errors from ERST register are accumulated here
0x14	-	-	0x0000	Unused
0x16	SYS	RW	0x0000	Audio processing controls
0x18	CTRL	WO	0x0000	Other controls
0x1A	-	RO	0x0000	Unused
0x1C	-	RO	0x0000	Unused
0x1E	-	RO	0x0000	Unused
0x20	VER	RO	0x5316	Digital Version
0x22	STAT	RO	0x0048	Copy of status byte at the beginning of current frame
0x24	CNT	RO	0x0000	Byte count from previous SPI frame
0x26	-	RO	0x0000	Unused
0x28	-	RO	0x0000	Unused
0x2A	-	RO	0x0000	Unused
0x2C	-	RO	0x0000	Unused
0x2E	-	RO	0x0000	Unused
0x30	SYSC	RW	0x0000	Chip can be enabled and disabled
0x32	AI	RO	0x?	Test register
0x34	GPIO	RO	0x0000	GPIO input digital signal read
0x36	-	RO	0x0000	Unused
0x38	BLKOVR	RW	0xX000	Revision ID and disables for various blocks
0x3A	TRIM	RW	0x0000	Disable internal oscillator, internal oscillator trim
0x3C	SRAM	RW	0x8000	SRAM block controls
0x3E	CTRL	RW	0x0000	Set SPI mode, external clock select, system reset

3.1.2 Indirect Registers

Table 3: Indirect Registers

Address	Name	Type	Reset	Description
0x0000	STM	RW	0x01400040	Startup calibration controls
0x0001	TDC	RW	0x00015C47	TDC controls
0x0002	AUD1	RW	0x1F801F8	Audio processing logic controls
0x0003	AUD2	RW	0x273F01F8	Audio processing logic controls
0x0004	TRM	RW	0x00000000	Trim controls
0x0005	TST	RW	0x00000000	Test mode selection
0x0006	AMX	RW	0x00000000	Signal routing and multiplexing controls
0x0007	AMB	RW	0x00FEFEFE	
0x0008	AMI	RW	0x00000000	Diagnostics for audio logic
0x0009	AMM	RW	0x00000000	Diagnostics for audio logic
0x000A	IOE	RW	0x00000000	Pin overrides
0x000B	IOD	RW	0x00000000	Pin overrides
0x000C	IOX	RW	0x00101010	Pin overrides
0x000D	SYSD	RW	0x00000000	Writes to SRAM
0x000E	AUDD	RW/RO	0x00400000	Audio processing logic controls
0x000F	AUDS1	RO	0x00000000	Diagnostics for audio logic
0x0010	AUDS2	RO	0x00000001	Diagnostics for audio logic
0x0011	AUDS3	RO	0x00FFFFFE	Diagnostics for audio logic
0x0012	FEX1	RW	0x00000000	Diagnostics for feature processing
0x0013	FEX2	RW/RO	0x00000000	Diagnostics for feature processing
0x0014	DRI	RO	0x00000000	Diagnostics for feature processing
0x0015	DSS	RO	0x00000000	Diagnostics for feature processing
0x0016	DCNT	RW/RO	0x00000000	Diagnostics for feature processing
0x0017	DMM	RW	0x000001FF	Diagnostics for feature processing
0x0018	DOPT	RW	0x00000000	Controls to output real-time feature data stream
0x0019	-	-	0x00000000	Unused
0x001A	-	-	0x00000000	Unused
0x001B	-	-	0x00000000	Unused
0x001C	PINR1	RW	0x00000000	GPIO signal routing
0x001D	PINR2	RW	0x00000000	GPIO signal routing
0x001E	TDCD	RW	0x00001000	TDC controls
0x001F	SPARE	RW	0x00020000	Configuration
0x0020	COEFF	RW	0x00000000	TDC sequencer logic
…	COEFF	RW	0x00000000	TDC sequencer logic
0x002F	COEFF	RW	0x00000000	TDC sequencer logic
0x0030 - 0x0FFF	-	RO	0x00000000	Unused
0x1000 - 0x13FF	PSD-SRAM	RW	0x?	PSD SRAM address range
0x1400 - 0x1FFF	PSD-SRAM	RW	0x?	Unused
0x2000 - 0x3FFF	ROM	RO	0x?	Specific default coefficients for feature extraction
0x4000 - 0x5FFF	COEFF-SRAM	RW	0x?	Custom coefficients can be uploaded and used
0x6000 - 0xFFFF	-	RO	0x00000000	Unused

4 SPI Slave

A SPI frame starts with falling CSN and is a minimum of 4 bytes for full completion of a register read or write. CSN rising before the end of the 4th byte will reset the SPI slave and possibly result in an incomplete transaction. Each register transaction is a 16-bit write or read to either a direct serial register. The SPI protocol can operate in either single or streaming mode. In the figures below, NOP stands for “No Operation”, as the SPI logic does not care what is transmitted in this time frame. The single-byte Status block at the beginning of each MISO SPI transmission returns either 0x48 or 0x49, if no errors are detected by the AIS2001 SPI block.

4.1 Single Write

The bytes on MOSI are reflected to MISO for data integrity checking. Data is written to the target register during the 3rd byte after the WriteCmd. If that byte was not present, the register write would not complete and a “WriteAbort”-error would be set in Status register.

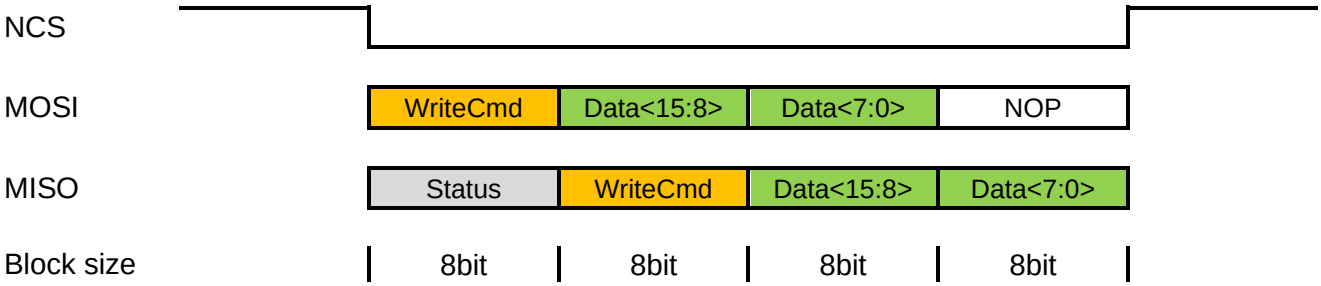


Figure 3: Single Write SPI transmission

4.2 Single Read

The ReadCmd byte on MOSI is reflected to MISO for data integrity checking. The 16-bit data from the register read is returned on MOSI in the 3rd and 4th bytes. The register read is done during the byte following the ReadCmd, giving sufficient time for synchronization to the system clock and data stabilization back to the SPI slave.

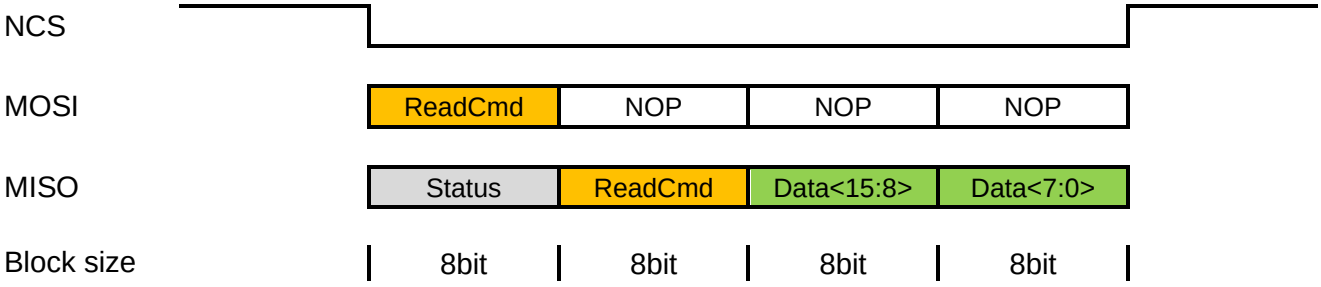


Figure 4: Single Write SPI transmission

4.3 Streaming Write

A new write command can be issued in place of the single command NOP, writing to another address. This can be continued as long as needed. It is not full streaming, but reduces the write overhead.

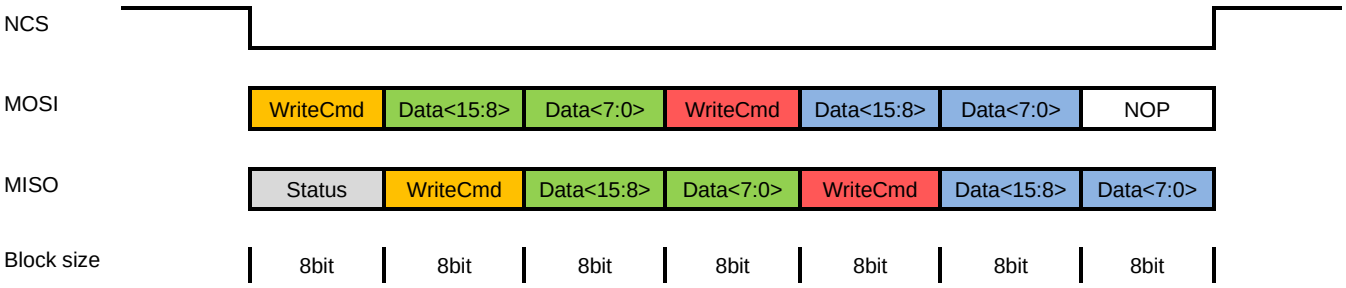


Figure 5: Streaming Write SPI transmission (two words shown)

4.4 Streaming Read

A new read command can be issued every other MOSI byte to continue receiving register data. This results in full streaming after the first two bytes in the frame.

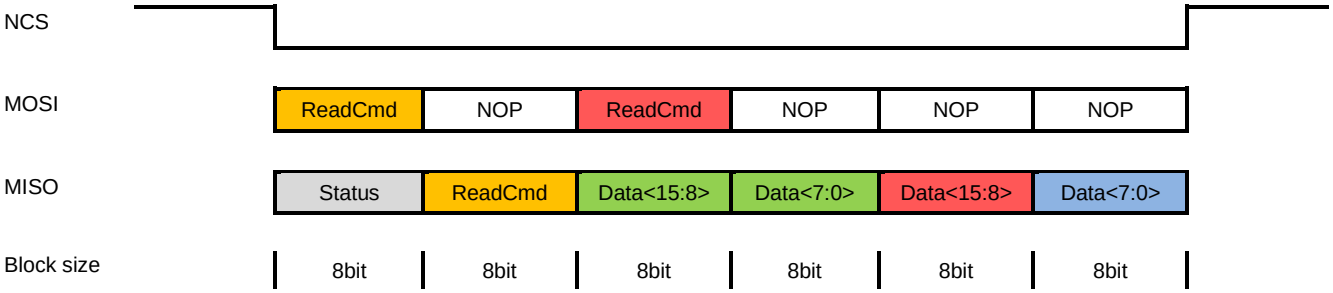


Figure 6: Streaming Read SPI transmission (two words shown)

4.5 Write Command format

The 8-bit WriteCmd block in the SPI transmission figures above is organized as follows:

bit	7	6	5	4	3	2	1	0
MOSI	1	0	Word Address					0

Figure 7: SPI Write Command format

4.6 Read Command format

The 8-bit ReadCmd block in the SPI transmission figures above is organized as follows:

bit	7	6	5	4	3	2	1	0
MOSI	0	1	Word Address					0

Figure 8: SPI Write Command format

5 Absolute Maximum Ratings[1]

Table 4: Absolute Maximum Ratings

ID	Pin	min	max	Unit	Condition
3.1	VIN Voltage	-0.3	4.3	V	
3.2	VAINP, VAINN Voltage	-0.3	VIN+0.3	V	
3.3	IOPR, IOPL Voltage	-0.3	VIN+0.3	V	
3.4	NCS, SCLK, MOSI, MISO Voltage	-0.3	VIN+0.3	V	
3.5	OUT1, GPIO1 - 6 Voltage	-0.3	VIN+0.3	V	
3.6	AVDD, DVDD Voltage	-0.3	1.35	V	
3.7	AGND, DGND, Exposed Pad Voltage	-0.3	0.3	V	
3.8	Operating Junction Temperature Range[2]	0	55	°C	
3.9	Storage Temperature Range	-40	135	°C	

6 Electrical Characteristics

6.1 Supply Voltage

Table 5: EC table Supply Voltage

ID	Parameter	Symbol	Typical	min	max	Unit	T_J[3]	Condition
4.1.1	VIN operating range	VIN		1.5	3.6	V	•	
4.1.2	Input operating current	I_{IN}	10 100 250		100 150 350	nA µA µA		AIS2001 Disabled AIS2001 Enabled, Audio Disabled AIS2001 Enabled, Audio Enabled

6.2 Power Supplies

Table 6: EC table Supply Voltage

ID	Parameter	Symbol	Typical	min	max	Unit	T_J[3]	Condition
4.2.1	AVDD Regulation Voltage	AVDD	1.22 1.22	1.21 1.19	1.23 1.25	V V	 •	T_A=25°C T_A=0°C to 55°C
4.2.2	DVDD Regulation Voltage	DVDD	1.22 1.22 1.10 1.10 1.00 1.00 0.90	1.21 1.19 1.09 1.07 0.99 0.97 0.88	1.23 1.25 1.11 1.13 1.01 1.03 0.92	V V V V V V V	 • • • •	TA=25°C, DVDD Select = 0 TA=0°C to 55°C, DVDD Select = 0 TA=25°C, DVDD Select = 1 TA=0°C to 55°C, DVDD Select = 1 TA=25°C, DVDD Select = 2 TA=0°C to 55°C, DVDD Select = 2 TA=0°C to 55°C, DVDD Select = 3
4.2.3	AVDD and DVDD Max DC Current	I_{VDD_max}	1			mA	•	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

[2] The AIS2001 is tested under pulsed load conditions such that TJ ≈ TA. The AIS2001 is guaranteed to meet specifications from 0 °C to 55°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The junction temperature (TJ) is calculated from the ambient temperature (TA) and power dissipation (PD) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$, where θ_{JA} is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

[3] The • denotes specifications that apply over the specified operating junction temperature range, otherwise specifications are at TA=25°C.[2] VIN=1.5V, unless otherwise noted.

4.2.4	AVDD and DVDD Supply Regulation		1.5			%		I_{VDD} = 500µA
4.2.5	AVDD and DVDD Load Regulation		1.5			%		I_{VDD} = 0µA to 1mA

6.3 Audio Characteristics

Table 7: EC table Supply Voltage

ID	Parameter	Symbol	Typical	min	max	Unit	T_J[3]	Condition
4.3.1	Audio Amplifier Gain	GMSEL	970 1900 266 29.5 324 627 89 9.9			µA/V µA/V µA/V µA/V µA/V µA/V µA/V µA/V		GM Select = 0 or 8 GM Select = 1 or 9 GM Select = 2 or 10 GM Select = 3 or 11 GM Select = 4 or 12 GM Select = 5 or 13 GM Select = 6 or 14 GM Select = 7 or 15
4.3.2	Maximum Peak Audio Input Range (Absolute Value of V_{AINP}-V_{AINN})		309 157 1.13 10.1 926 478 3.37 30.3			µV µV mV mV µV µV mV mV		GM Select = 0 or 8 GM Select = 1 or 9 GM Select = 2 or 10 GM Select = 3 or 11 GM Select = 4 or 12 GM Select = 5 or 13 GM Select = 6 or 14 GM Select = 7 or 15
4.3.3	Audio Amplifier Bandwidth		3.9 2.0 12.5 49.1 3.8 2.0 12.1 46.5 7.8 4.0 25.4 113.6 7.2 3.7 23.4 98.9			kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz kHz		GM Select = 0 GM Select = 1 GM Select = 2 GM Select = 3 GM Select = 4 GM Select = 5 GM Select = 6 GM Select = 7 GM Select = 8 GM Select = 9 GM Select = 10 GM Select = 11 GM Select = 12 GM Select = 13 GM Select = 14 GM Select = 15
4.3.4	Audio Sampling Frequency	$f_{Sampling}$	16.0 8.00	15.5 7.76	16.5 8.24	kHz kHz	• •	Programmed for 16kHz [4] Programmed for 8kHz [4]
4.3.5	Feature Frame Size		512			Samples		
4.3.6	Feature Stride Size		256			Samples		
4.3.7	Pre-Programmed Feature Frequency Bins at 16kHz Sample Rate [4] [5]		62.5 125.0 187.5 250.0 312.5 406.3 500.0 593.8 687.5 812.5			Hz Hz Hz Hz Hz Hz Hz Hz Hz Hz		Bin 0 Bin 1 Bin 3 Bin 4 Bin 5 Bin 6 Bin 7 Bin 8 Bin 9 Bin 10

[4] Consults Applications Information section for register settings and programming details for the AIS2001.
[5] Guaranteed by design. Not tested

			906.3			Hz		Bin 11
			1.063			kHz		Bin 12
			1.188			kHz		Bin 13
			1.344			kHz		Bin 14
			1.500			kHz		Bin 15
			1.688			kHz		Bin 16
			1.875			kHz		Bin 17
			2.063			kHz		Bin 18
			2.531			kHz		Bin 19
			2.781			kHz		Bin 20
			3.063			kHz		Bin 21
			3.344			kHz		Bin 22
			3.688			kHz		Bin 23
			4.031			kHz		Bin 24
			4.406			kHz		Bin 25
			4.813			kHz		Bin 26
			5.250			kHz		Bin 27
			5.719			kHz		Bin 28
			6.219			kHz		Bin 29
			6.781			kHz		Bin 30
			7.375			kHz		Bin 31

6.4 I/Os

Table 8: EC table I/Os

ID	Parameter	Symbol	Typical	min	max	Unit	T_J[3]	Condition
4.4.1	Digital Input Rising Threshold				75	% of VIN	•	
4.4.2	Digital Input Falling Threshold			25		% of VIN	•	
4.4.3	Digital Input Leakage Current		10		30	nA		
4.4.4	Digital Output Pull-Up Resistance		15		50	Ω	•	VIN-V_{GPIO}=0.2V, I_{GPIO}=1mA
4.4.5	Digital Output Pull-Down Resistance		6		25	Ω	•	V_{GPIO}=0.2V, I_{GPIO}=1mA
4.4.6	Maximum SPI Clock Frequency		8			MHz	•	

7 Typical Application

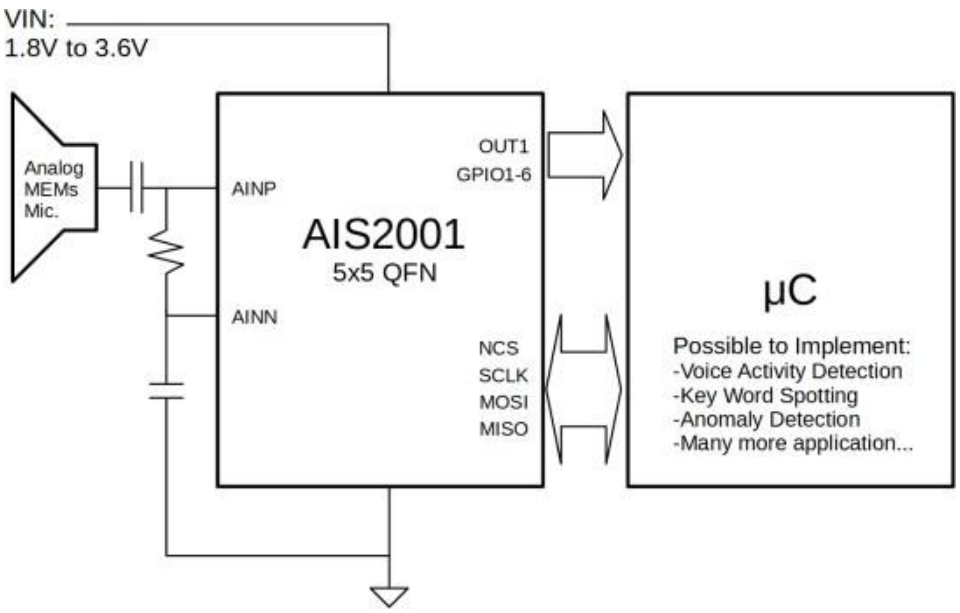


Figure 9: Typical Application

8 Board Layout Considerations

AGND (Pins 2,3,4): Analog ground pins. Connect all three pins together at the AIS2001, and kelvin all AVDD, VIN, and AINN bypass capacitors to these pins. Make a single connection from these pins to board ground for the best noise performance.

AINN (Pin 5): Inverting input of the input audio amplifier. Bypass this pin to AGND with a recommended 44µF of capacitance and connect a recommended 4.7kΩ resistor between this pin and AINP.

IOPL (Pin 6): Analog output of the input audio amplifier that can be used for RMS level detection or Automatic Gain Control. See the Applications Information section for details.

AINP (Pin 7): Non-inverting input of the input audio amplifier. Couple the single ended analog audio signal to this pin through a recommended 22µF of capacitance.

GPIO1 (Pin 9): General purpose digital output. This pin can be driven up to VIN.

IOPR (Pin 10): Analog output of the input audio amplifier that can be used for RMS level detection or Automatic Gain Control. See the Applications Information section for details.

GPIO2-6 (Pin 11,12,13,15,16): General purpose digital output. This pin can be driven up to VIN.

OUT1 (Pin 14): General purpose digital output. This pin can be driven up to VIN.

SCLK (Pin 18): Clock input of the SPI interface. MOSI (Pin 20): MOSI input of the SPI interface.

MISO (Pin 22): MISO input of the SPI interface. NCS (Pin 24): Chip select of the SPI interface.

DGND (Pin 25): Digital ground pin. The DVDD bypass capacitor should be kelvined to this pin. Make a single connection from this pin to board ground for the best noise performance.

DVDD (Pins 26,27,28): AIS2001 generated digital supply voltage. Connect all pins together at the AIS2001 and bypass with a minimum of 1µF to the DGND pin.

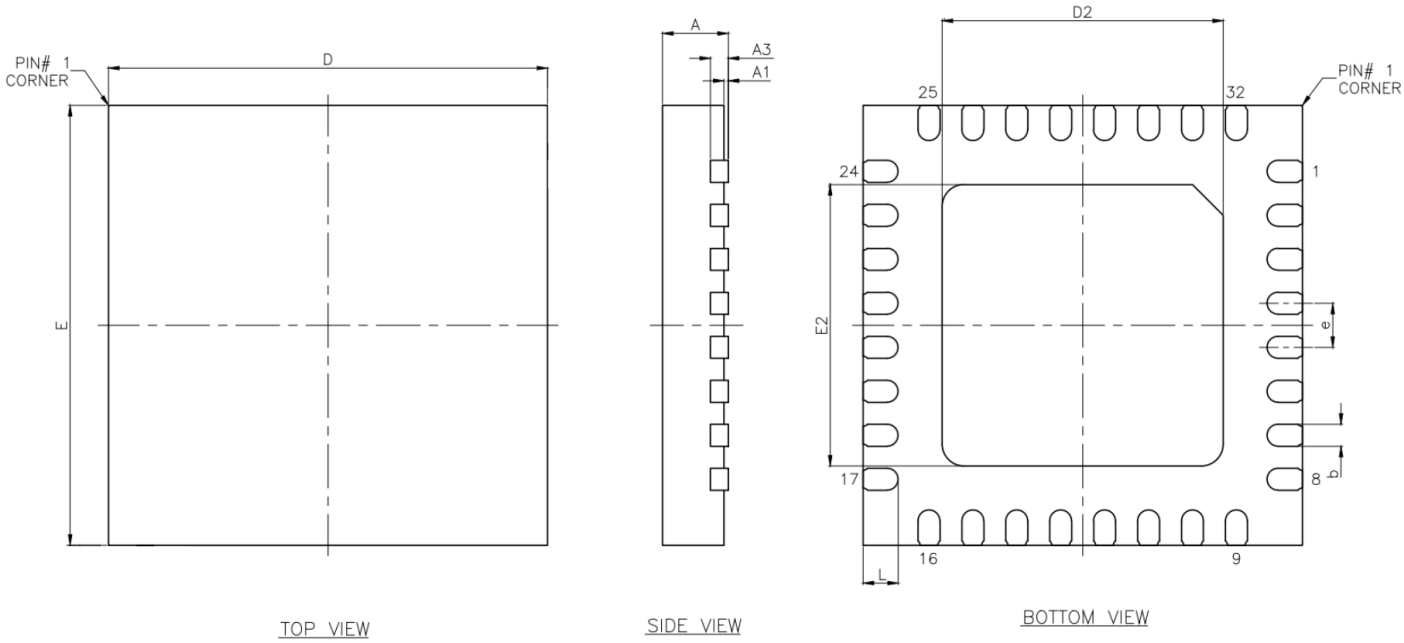
VIN (Pins 29,30): Input voltage to the AIS2001. Connect all pins together at the AIS2001 and bypass with a minimum of 1µF to the AGND pin.

AVDD (Pins 31,32): AIS2001 generated analog supply voltage. Connect all pins together at the AIS2001 and bypass with a minimum of 1µF to the AGND pin.

NC (Pins 1,8,17,19,21,23): No connect pins. These pins have no electrical connections but must still be soldered to the PCB for mechanical strength.

Exposed Pad (Pin 33): This pin has no electrical connection but must be soldered to ground for mechanical strength and thermal performance.

9 Package Information



	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Lead thickness	A3	0.20 REF.		
Body size	D	4.90	5.00	5.10
	E	4.90	5.00	5.10

BBD no	Pad size	Lead width b			Exposed pad width D2			Exposed pad length E2			Lead pitch e	Lead length L			LEAD FINISH	
		MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.		MIN.	NOM	MAX.	Pure Tin	PPF
BBDPQAA032-001	151x151MIL	0.20	0.25	0.30	3.10	3.20	3.30	3.10	3.20	3.30	0.50 BSC	0.30	0.40	0.50	V	X

Figure 10: Package Information of WQFN 32Pin Package

10 List of Abbreviations

Table 9: List of Abbreviations

Name	Description
GPIO	General Purpose I/O
I/O	Input-Output
MEMS	Micro-Electromechanical Systems
PSD	Power Spectral Density
ROM	Read-Only Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory

11 Revision History

Table 10: Revision History

Revision	Date	Description	Author
0.1	2025-03-19	Initial revision	Maximilian Heindel

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14 Important Notice and Disclaimer

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3. Ensure that your application complies with applicable standards and meets all safety, security, regulatory, and other requirements.

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